

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Adrian P. Wise

Filed: February 6, 2001

For: MULTISTANDARD VIDEO
DECODER AND DECOMPRESSION

SYSTEM FOR PROCESSING

ENCODED BIT STREAMS INCLUDING A §

DECODER WITH TOKEN GENERATOR §

AND METHODS RELATING THERETO §

§

§

§

§

§

§

§

§

§

§

§

Application No.: Not Yet Known

Art Unit: 2783 (anticipated)

Examiner: Follansbee, J. (anticipated)

Attorney Docket No.:

94100420(EP)USC1X1C1D9 PDDD

1033 U.S. PTO
09/777283
02/06/01

COMMUNICATION - SUBMISSION OF FORMAL DRAWINGS

BOX PATENT APPLICATION

Assistant Commissioner of Patents

Washington DC 20231

Sir:

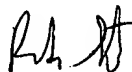
FILING OF CORRESPONDENCE BY EXPRESS MAIL UNDER 37 C.F.R. § 1.10	
EL443264310US	2/6/01
Express Mail Label Number	Date of Deposit

Transmitted herewith are 169 formal drawings on 124 sheets.

In the event a fee is due, the Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment to Deposit Account No. 04-1175.

Respectfully submitted,

DISCOVISION ASSOCIATES



Richard Stokey
Reg. No. 40,383

Date: 2/6/01

DISCOVISION ASSOCIATES

INTELLECTUAL PROPERTY DEVELOPMENT

P.O. Box 19616

Irvine, California 92623

(949) 660-5006

RS:sd

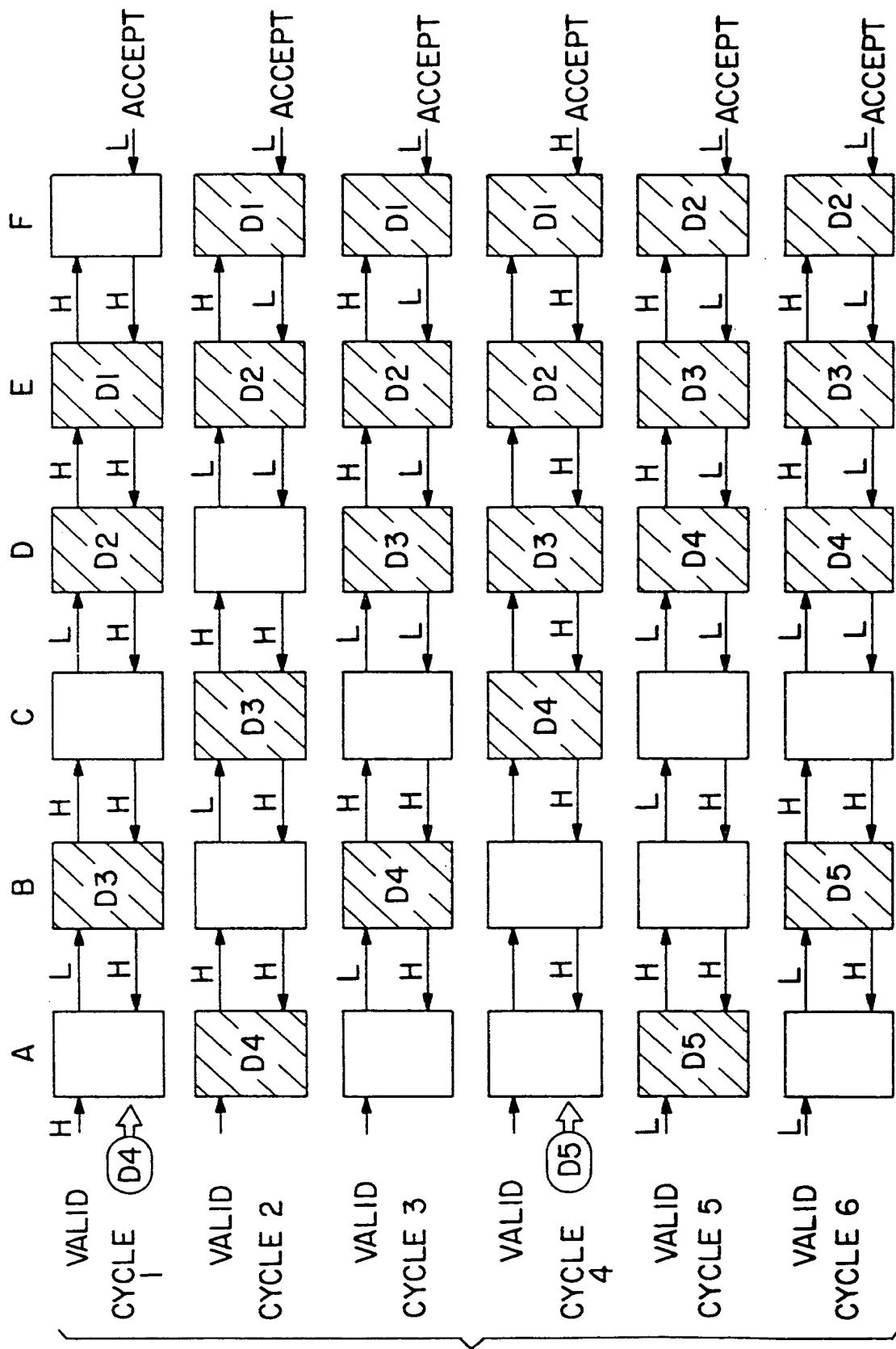


FIG. 1

The diagram illustrates the timing of a 3-stage pipeline (A, B, C) over six cycles. Each stage is represented by a box divided into two horizontal sections. Arrows indicate the flow of data and control signals between stages and to/from the external environment.

- Control Signals:**
 - VALID:** A signal that becomes valid at the start of a cycle and remains valid until the end of the cycle.
 - ACCEPT:** A signal that is asserted at the start of a cycle and deasserted at the end of the cycle.
- Data Flow:**
 - D4:** Data 4 is processed in Stage A during Cycle 1, Cycle 2, and Cycle 3.
 - D5:** Data 5 is processed in Stage A during Cycle 4, Cycle 5, and Cycle 6.
 - D3:** Data 3 is processed in Stage B during Cycle 1, Cycle 2, and Cycle 3.
 - D4:** Data 4 is processed in Stage B during Cycle 3, Cycle 4, and Cycle 5.
 - D5:** Data 5 is processed in Stage B during Cycle 5 and Cycle 6.
 - D2:** Data 2 is processed in Stage C during Cycle 1, Cycle 2, and Cycle 3.
 - D3:** Data 3 is processed in Stage C during Cycle 3, Cycle 4, and Cycle 5.
 - D4:** Data 4 is processed in Stage C during Cycle 5 and Cycle 6.

FIG. 2(A)

3

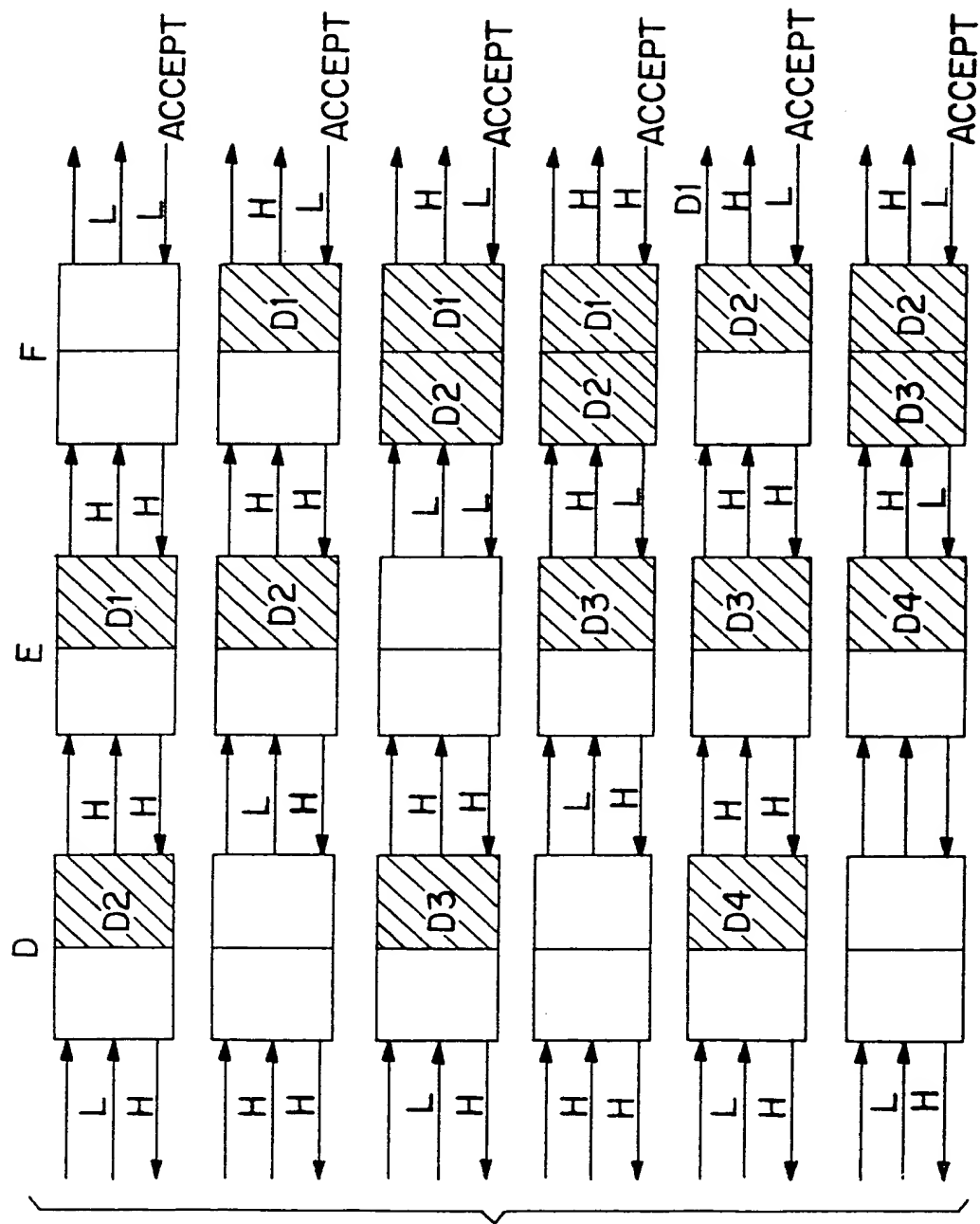


FIG. 2(B)

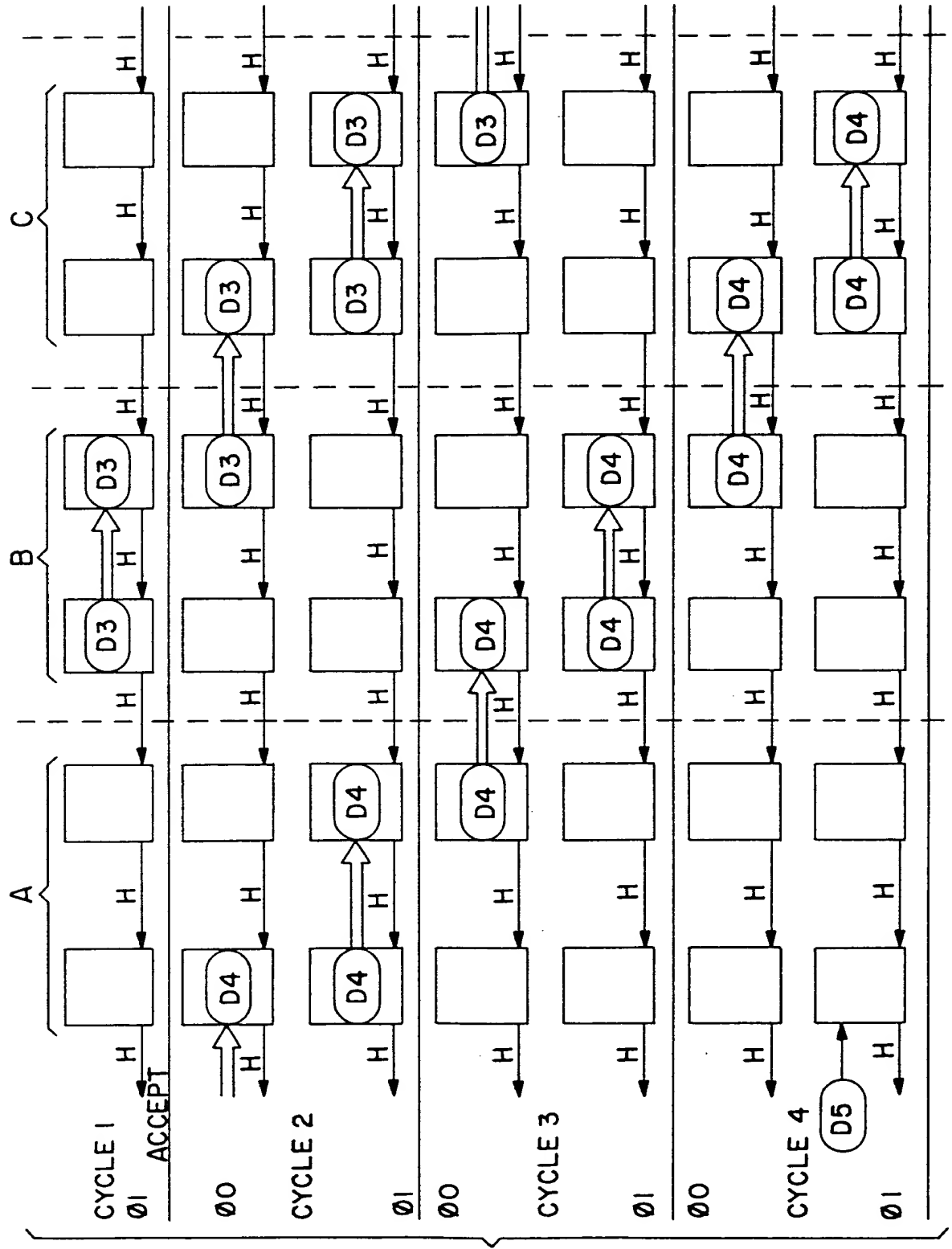


FIG. 3A-1

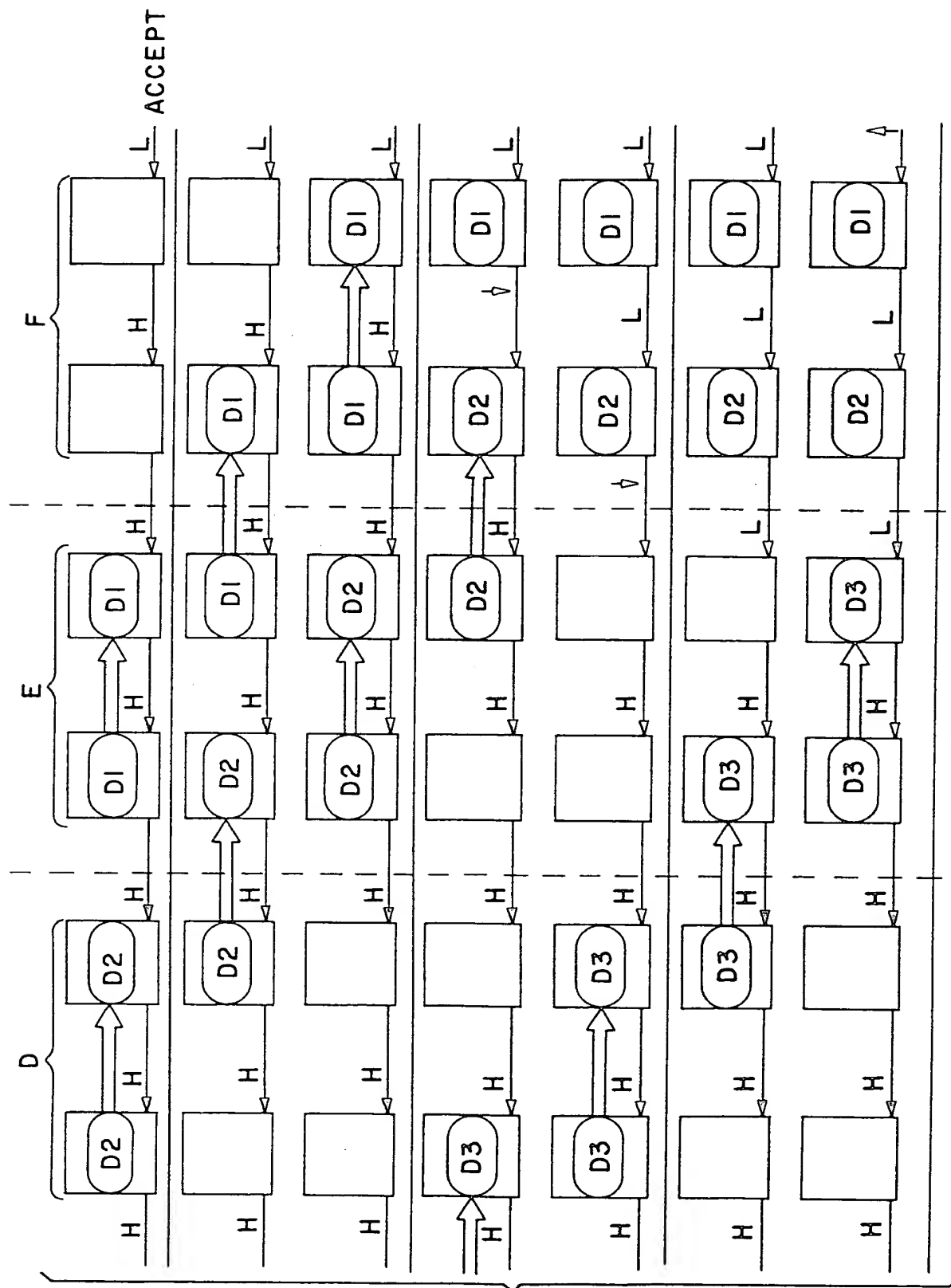


FIG. 3A-2

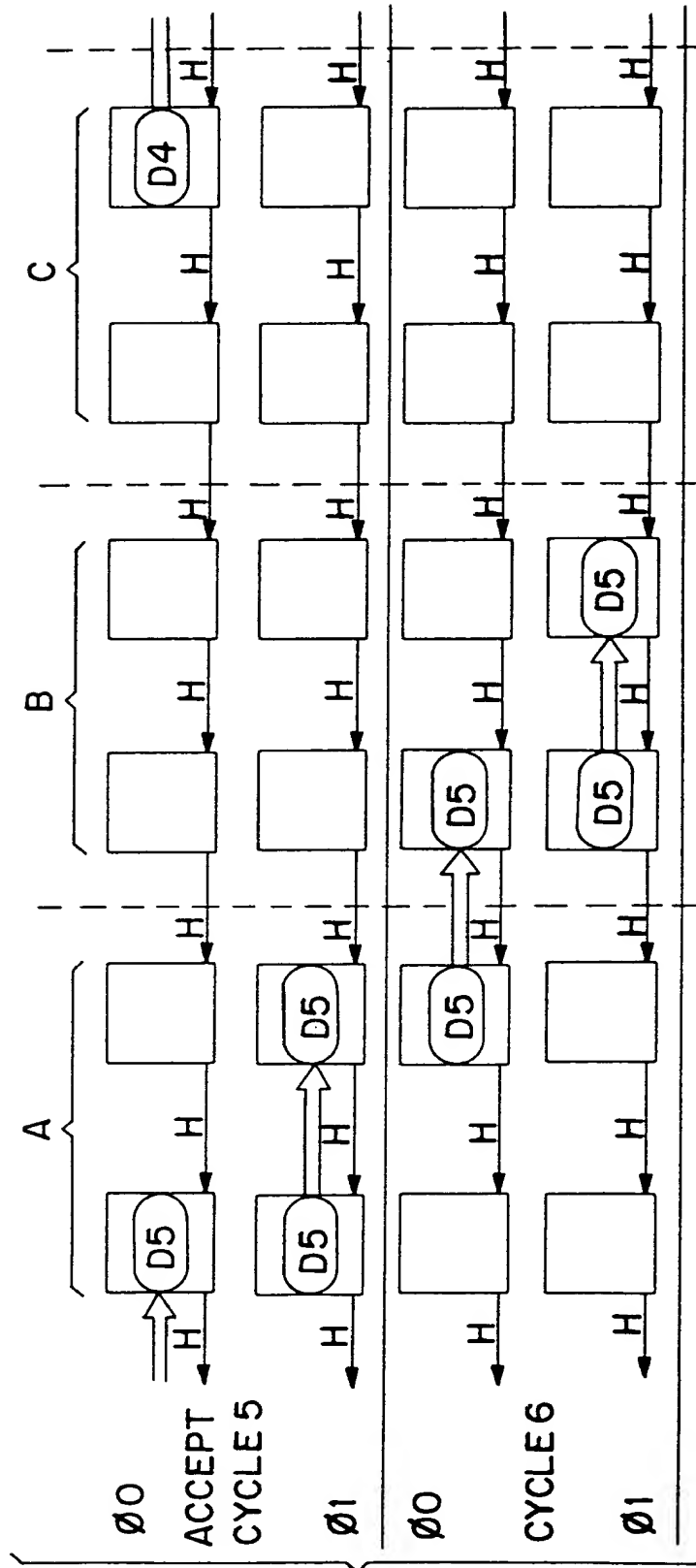


FIG. 3B-1

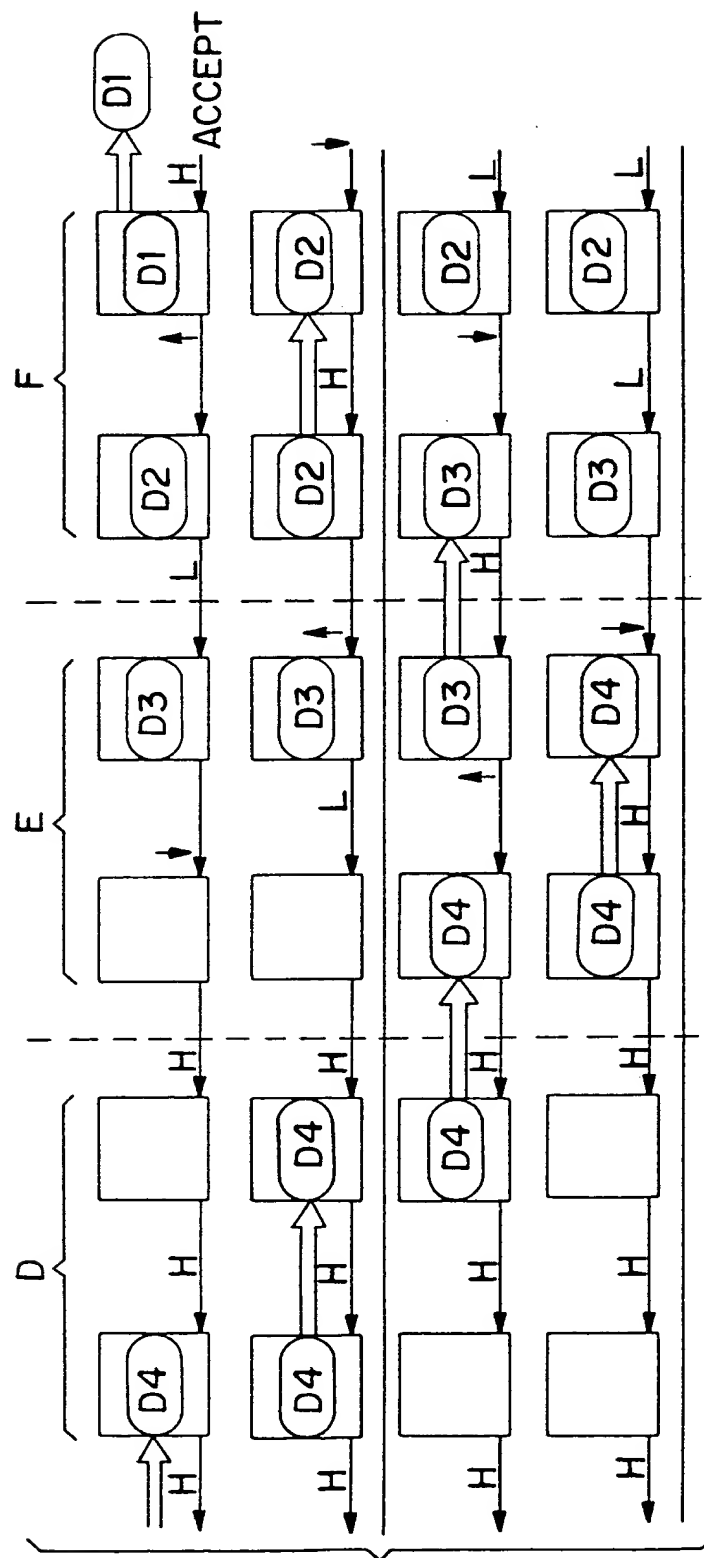


FIG. 3B-2

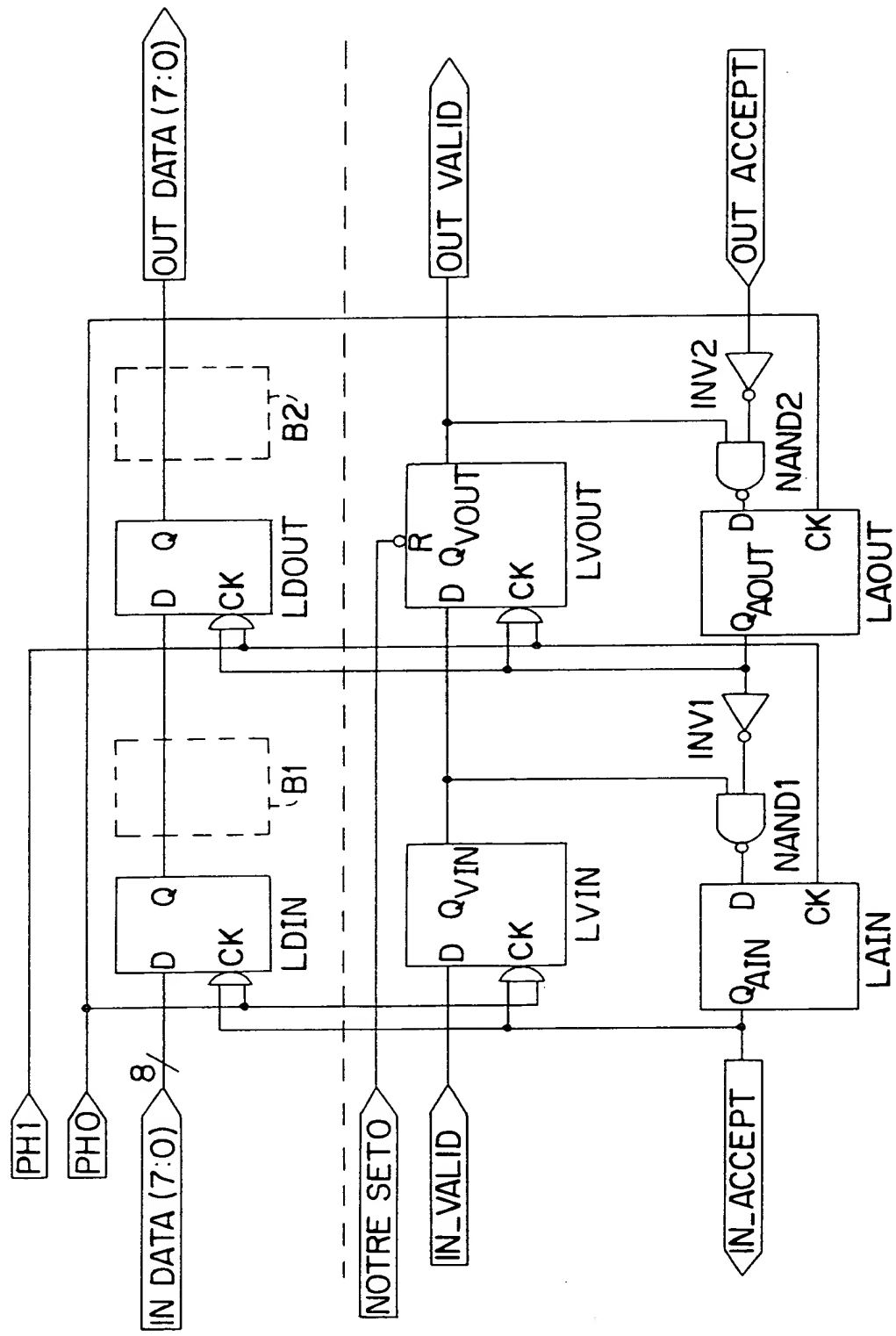


FIG. 4

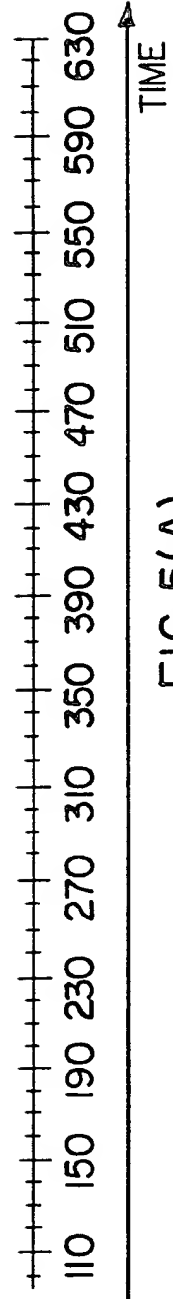
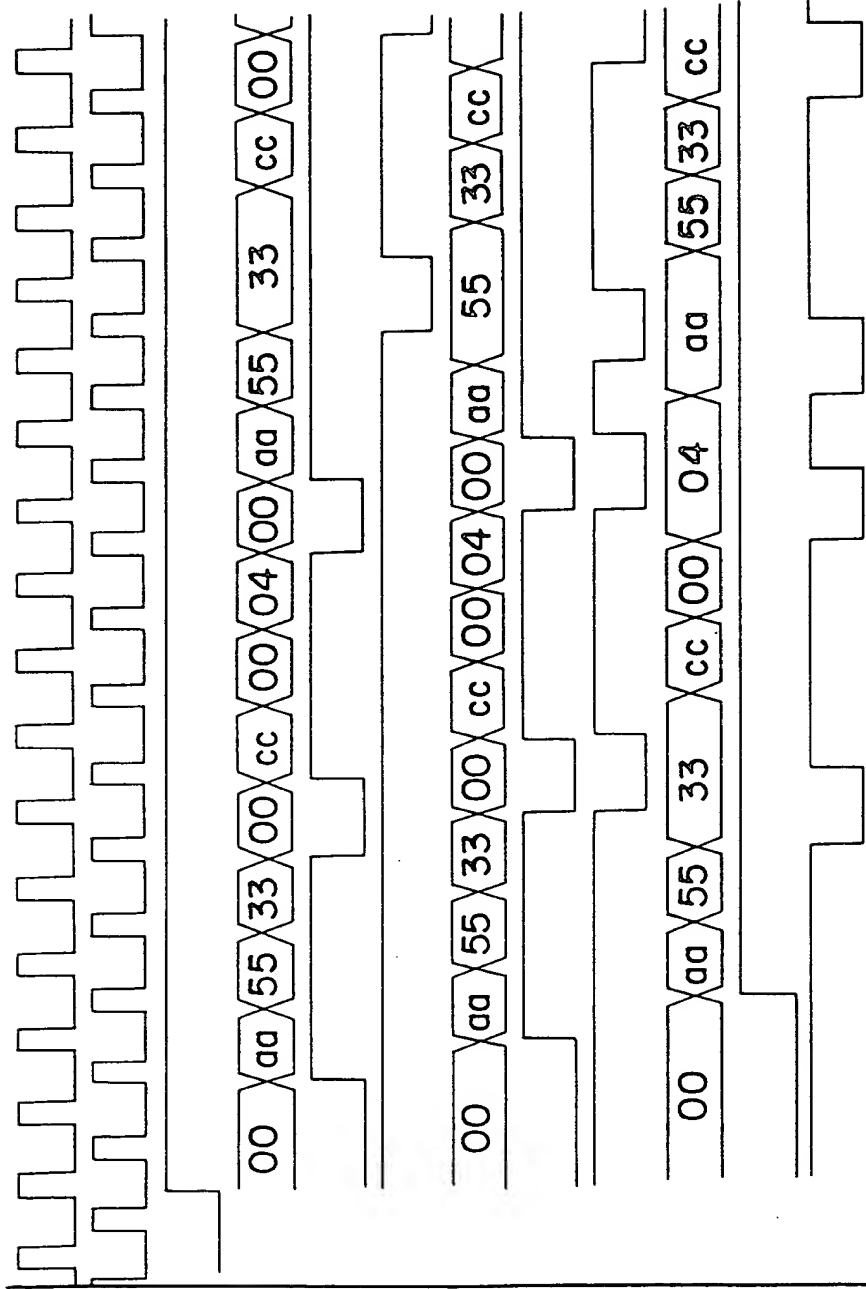


FIG. 5(A)

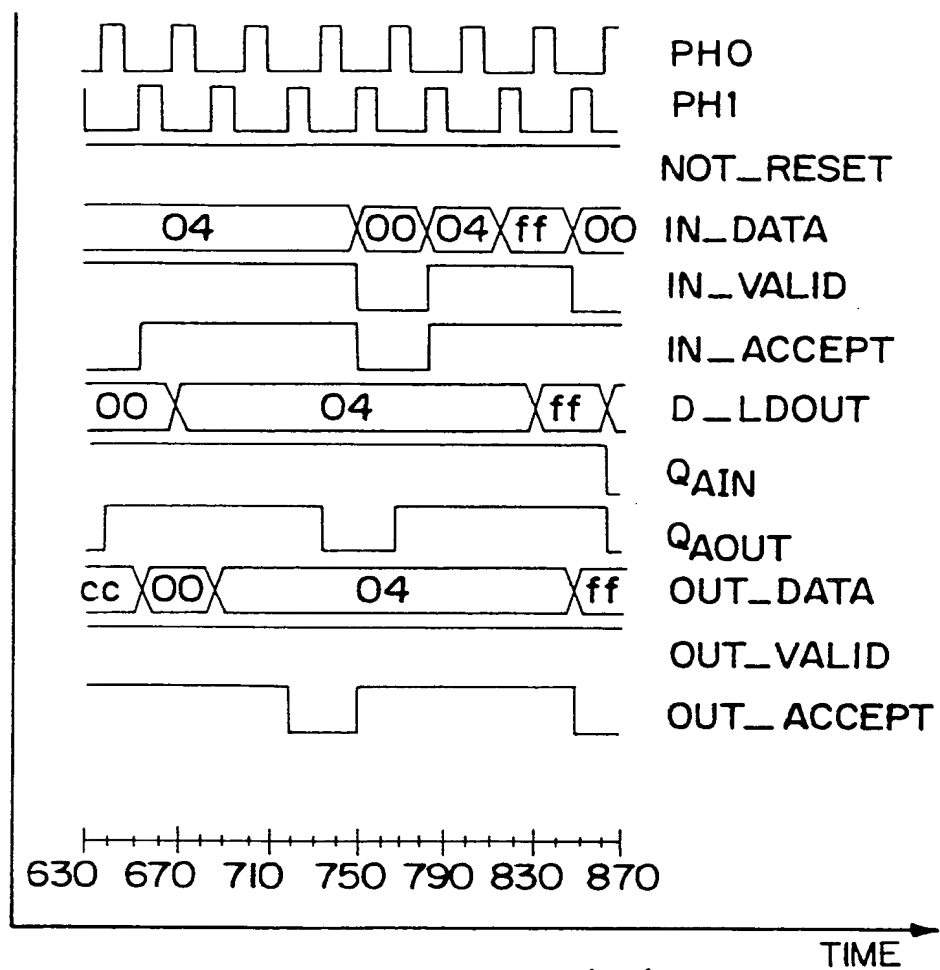


FIG. 5(B)

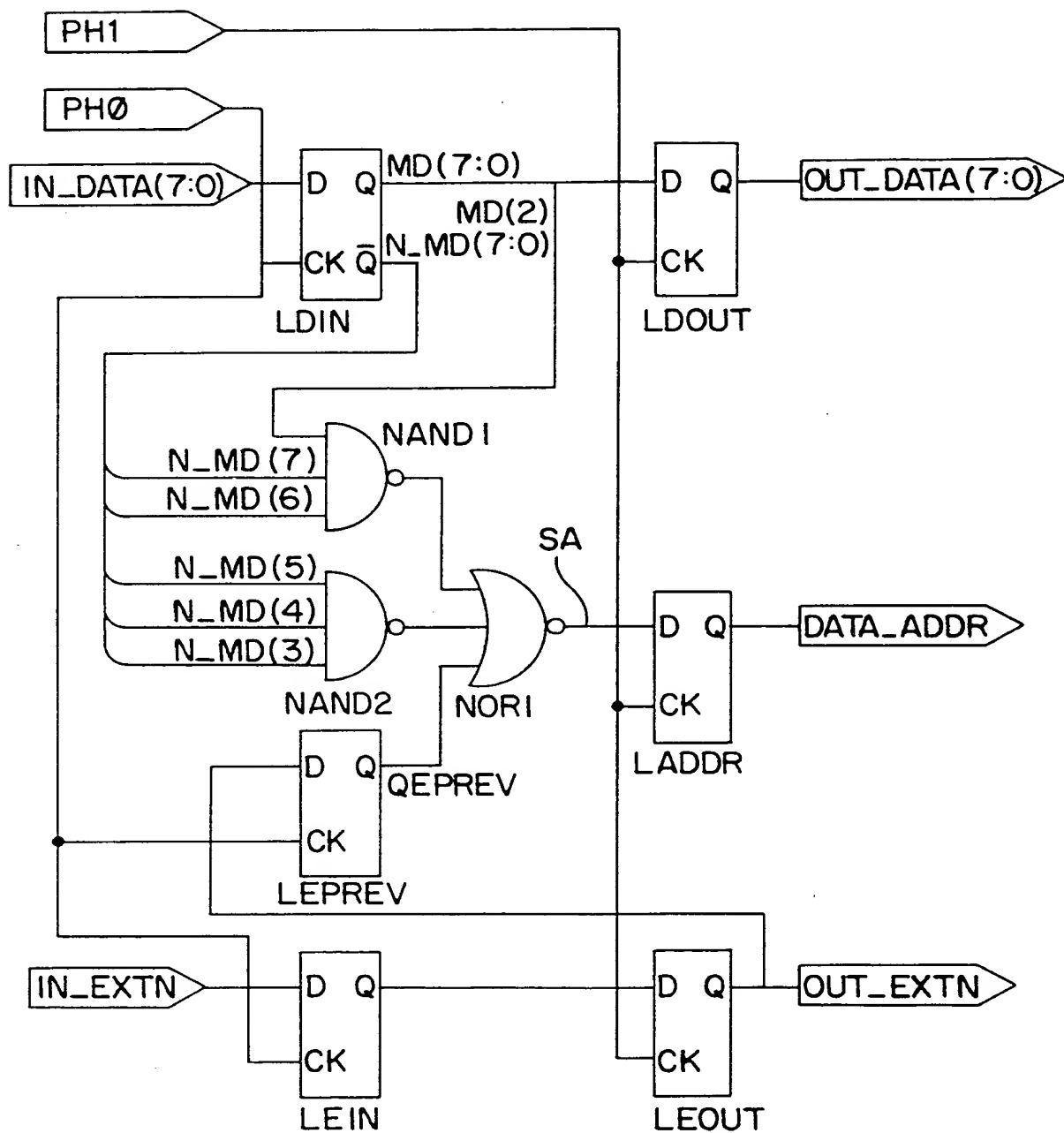


FIG. 6

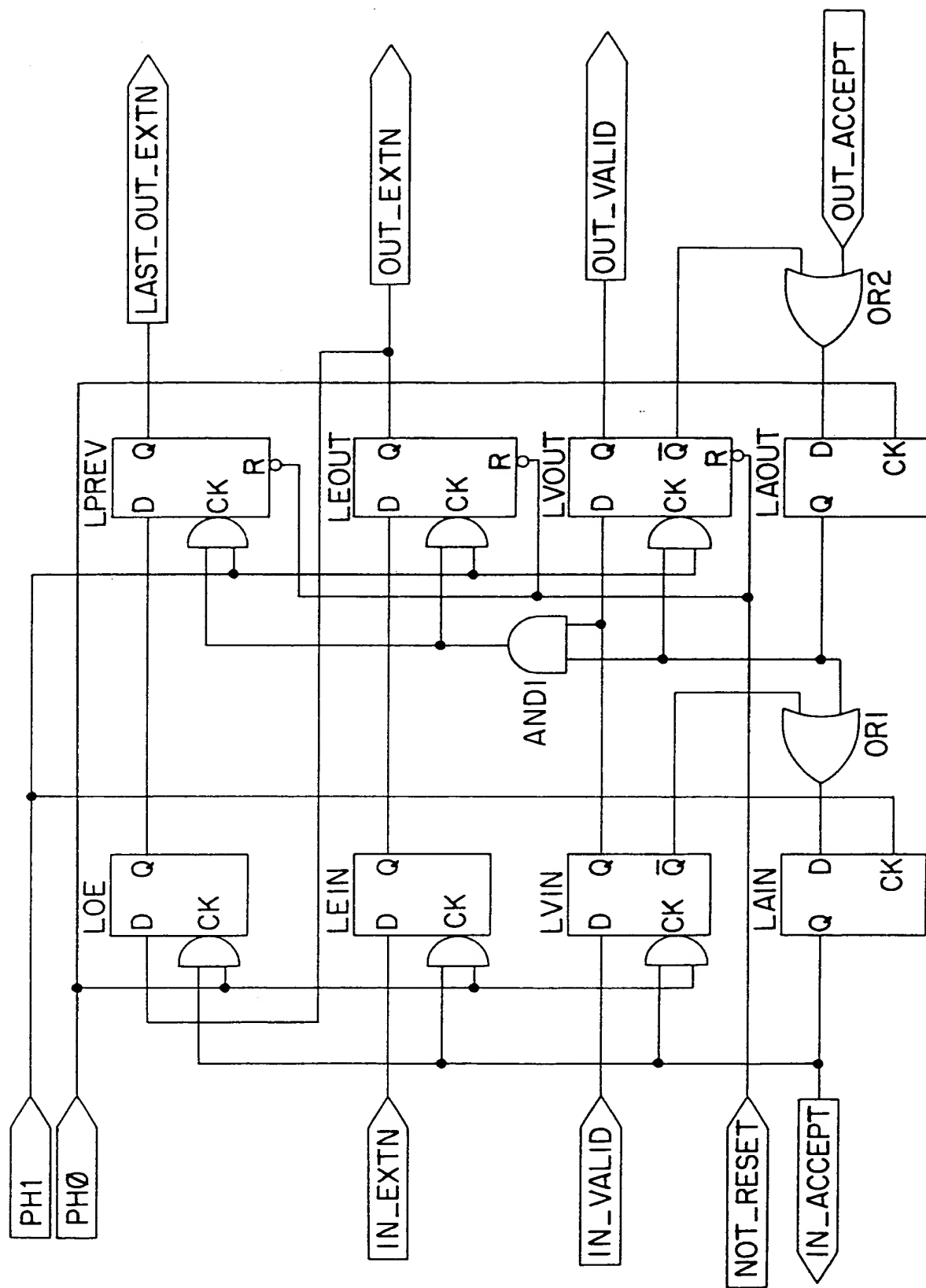


FIG. 7

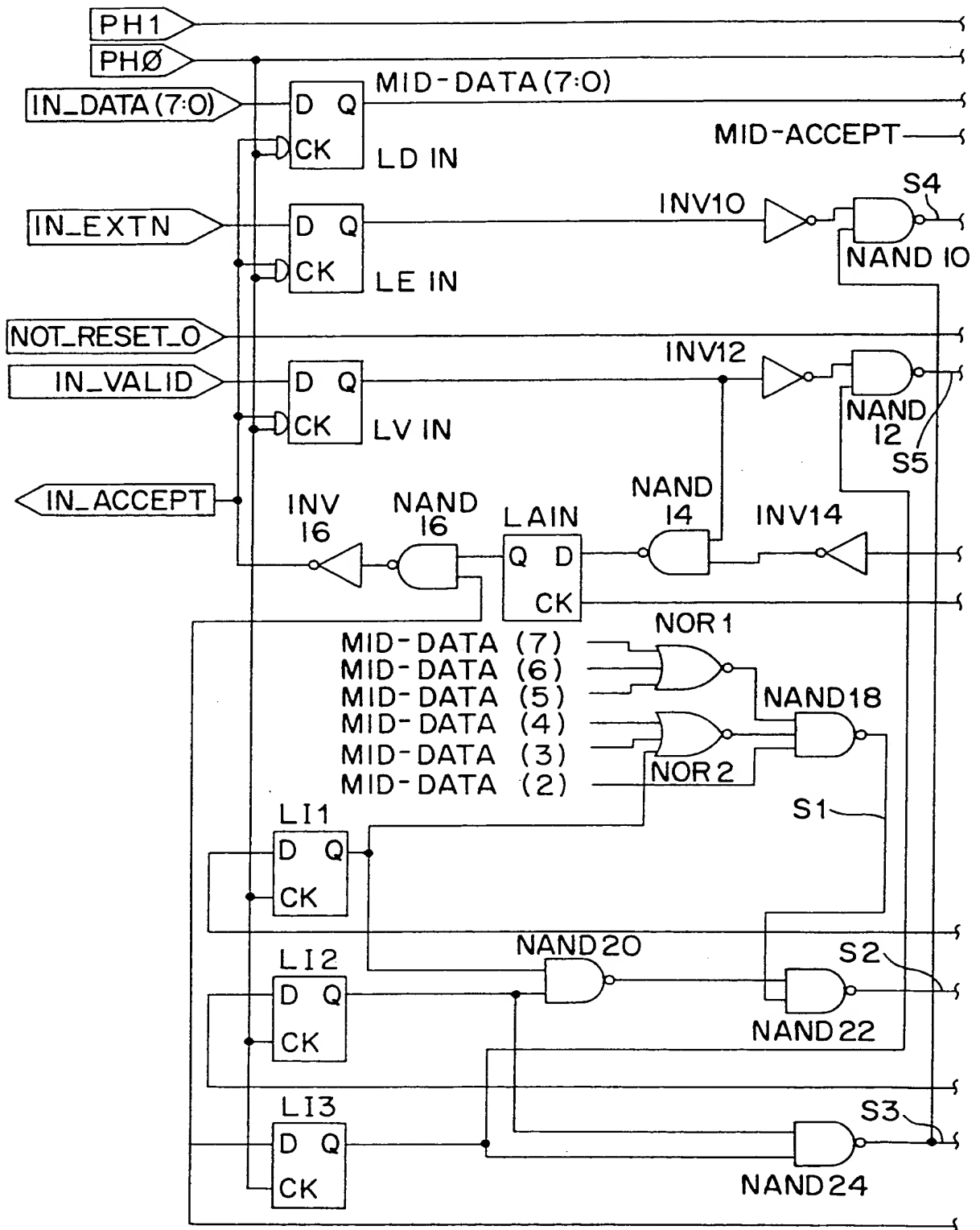


FIG. 8(A)

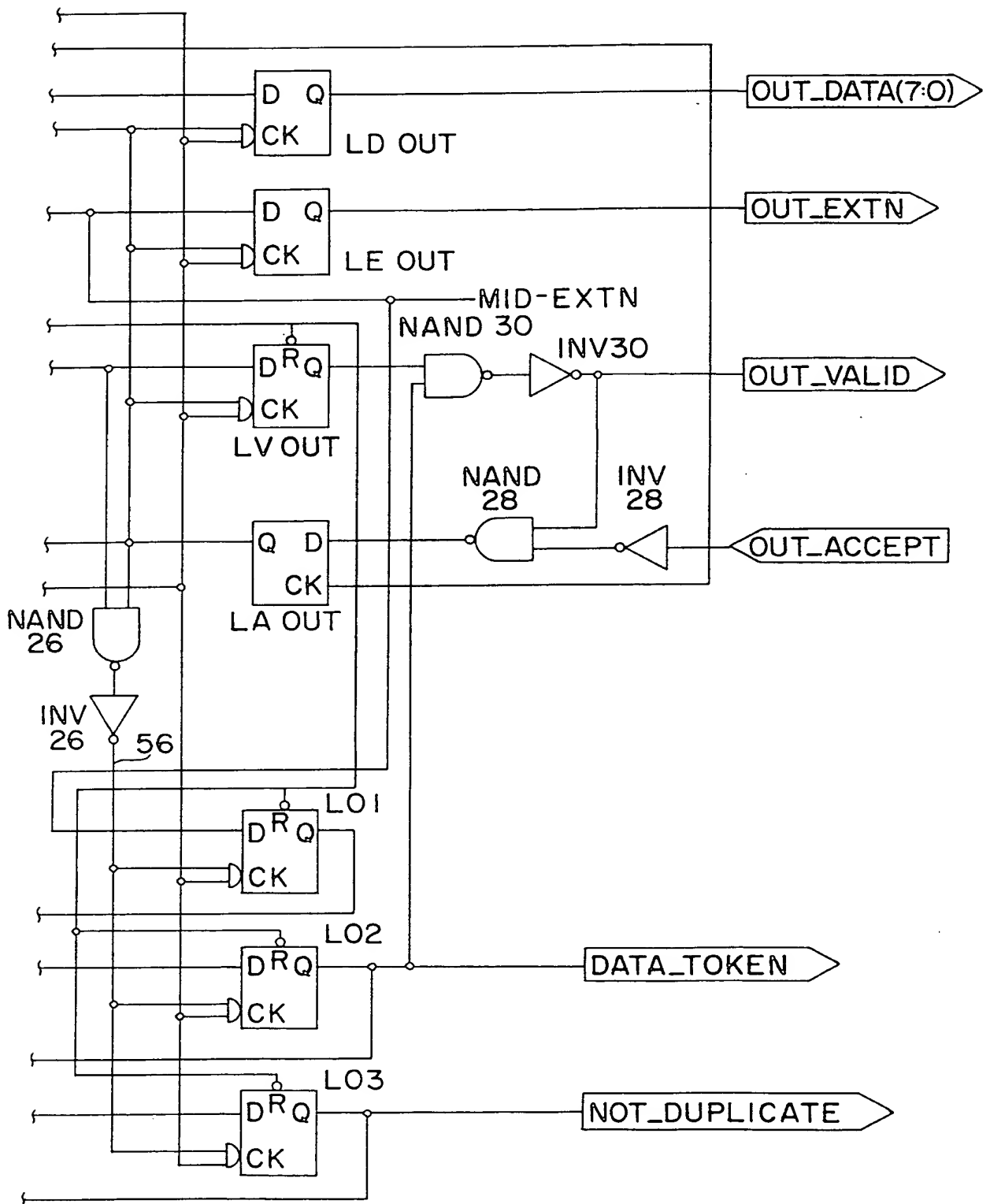


FIG. 8(B)

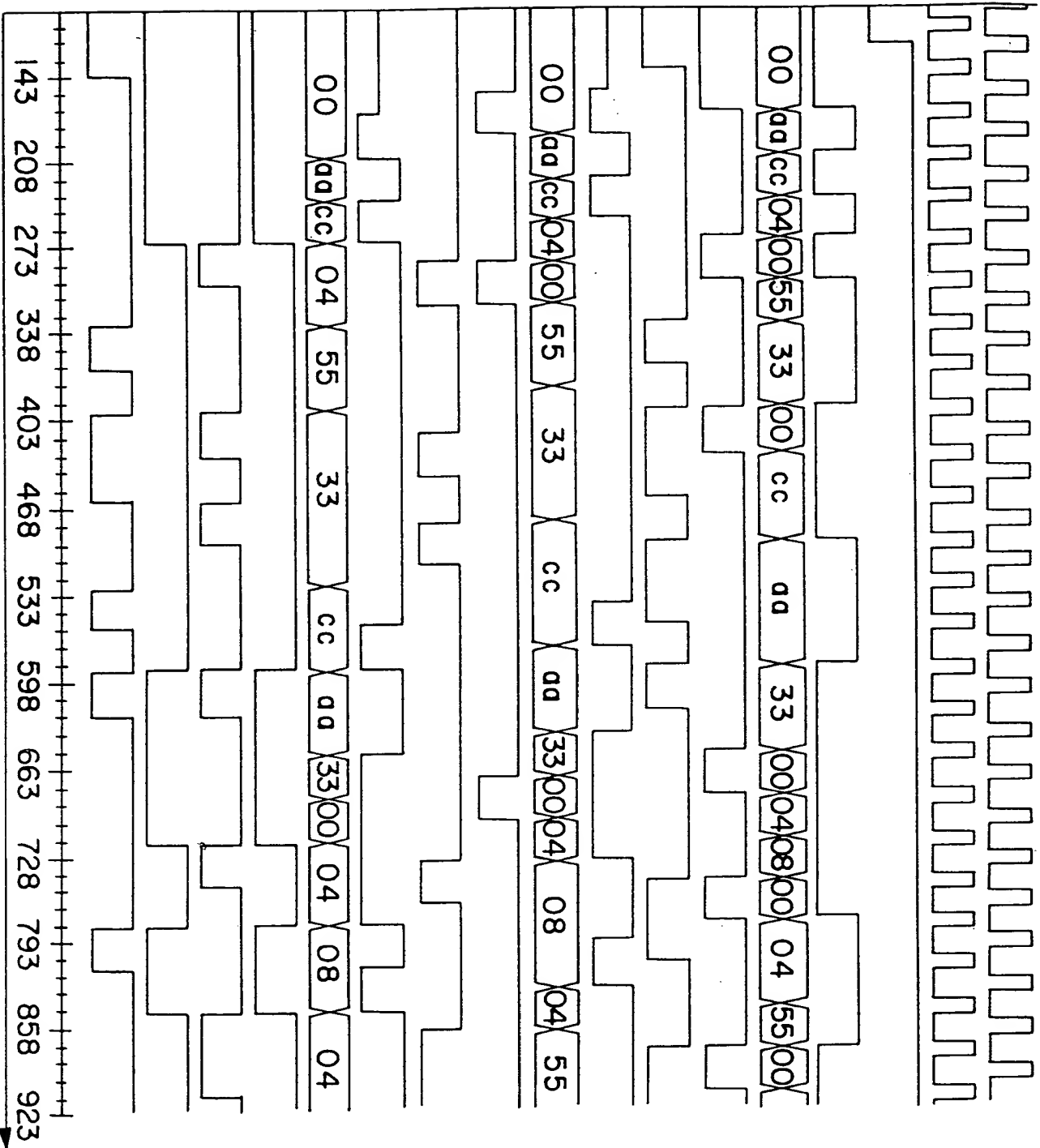


FIG. 9(A)

TIME

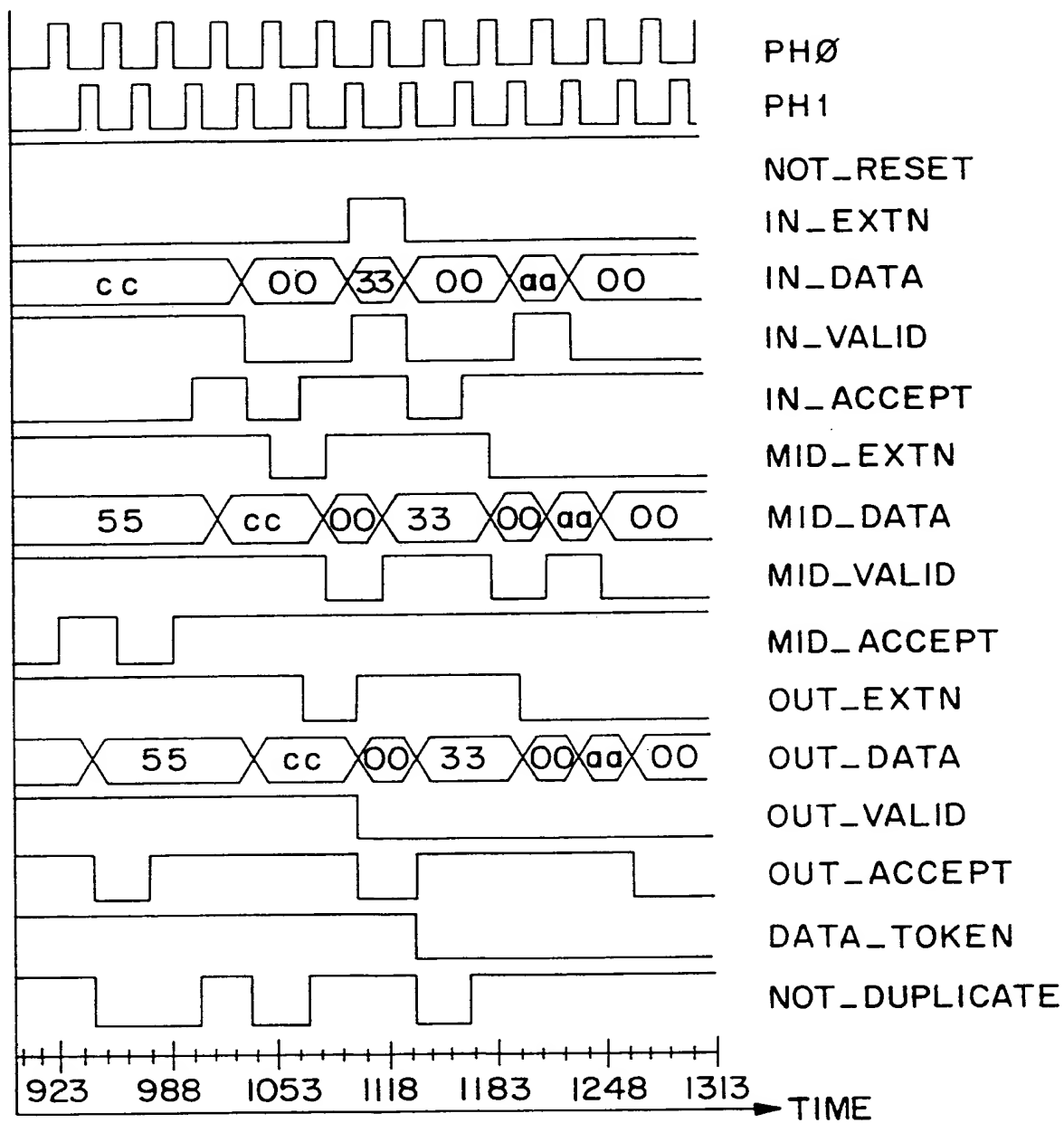


FIG. 9(B)

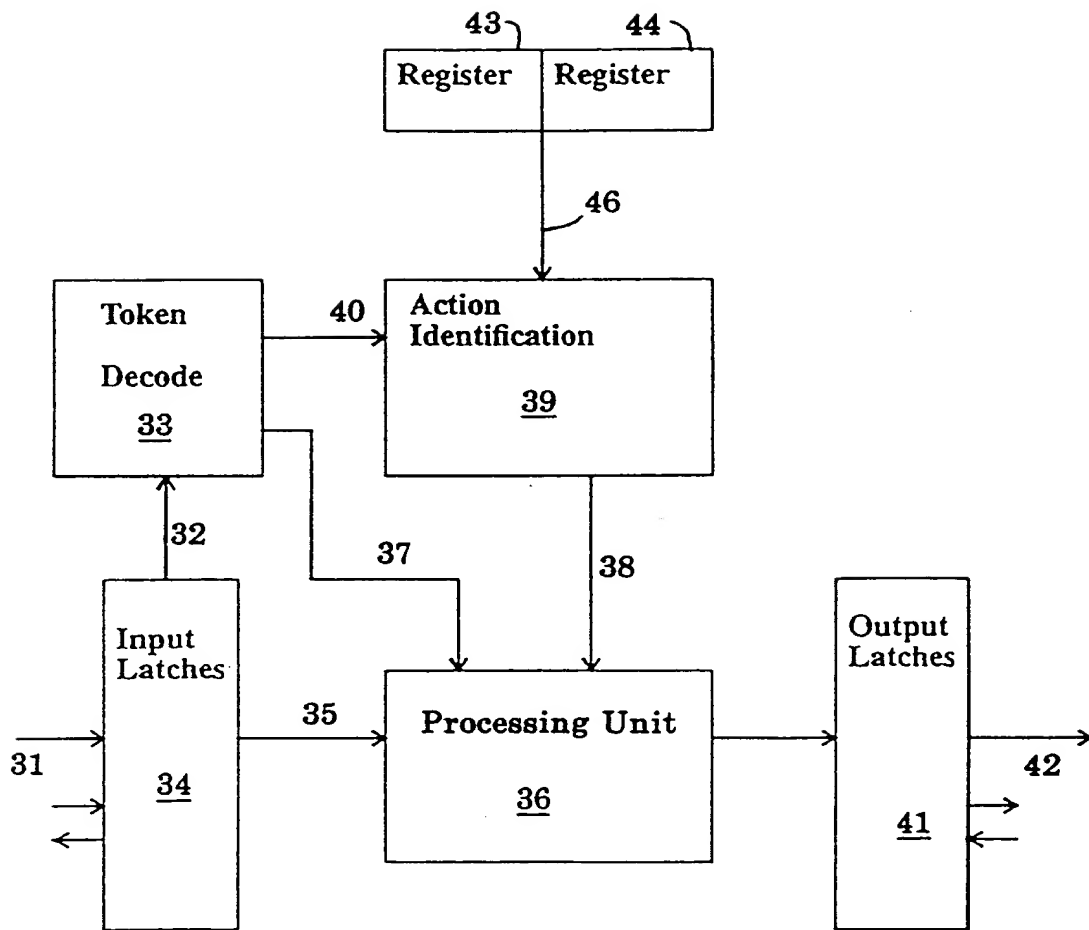


FIG. 10

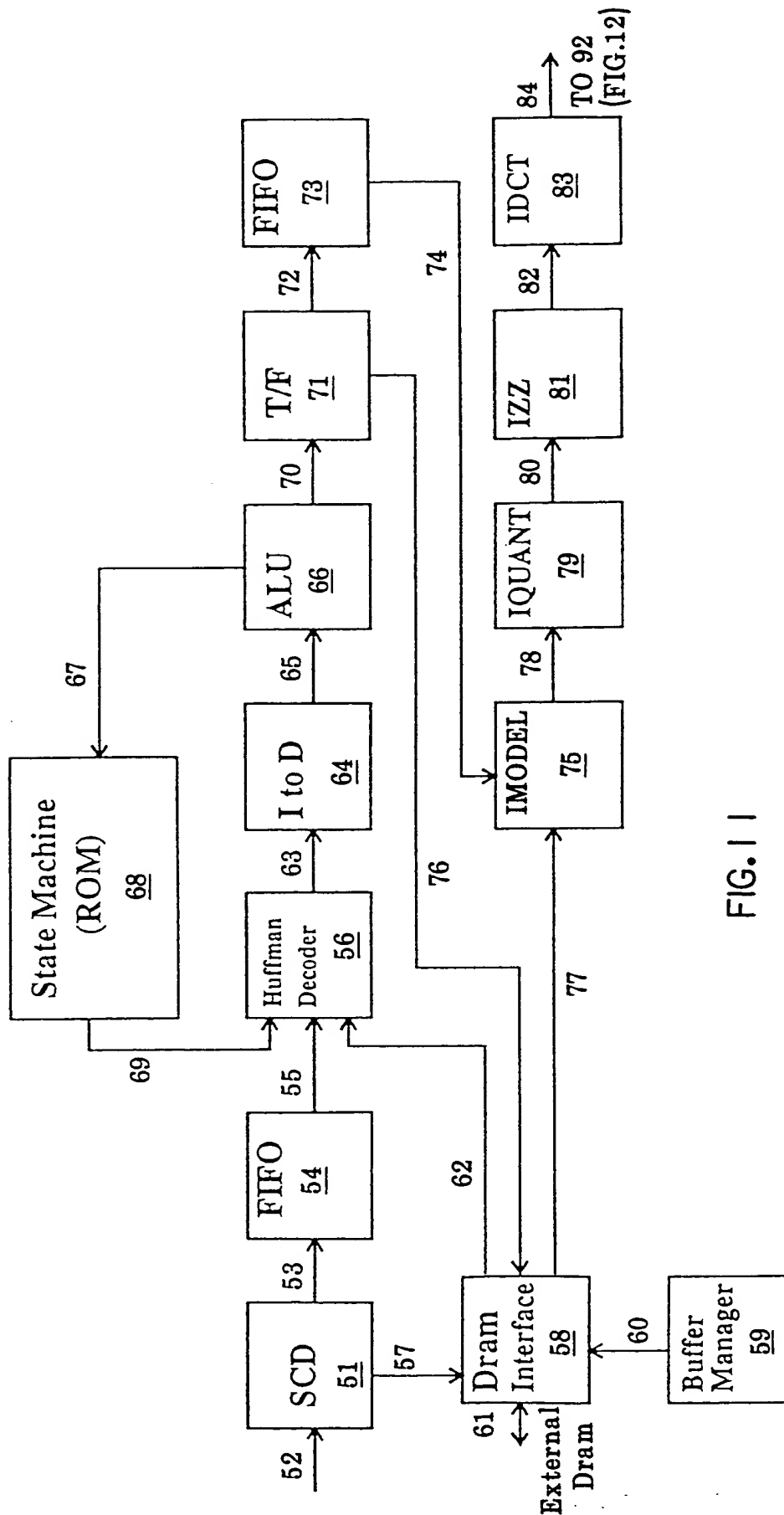


FIG. 11

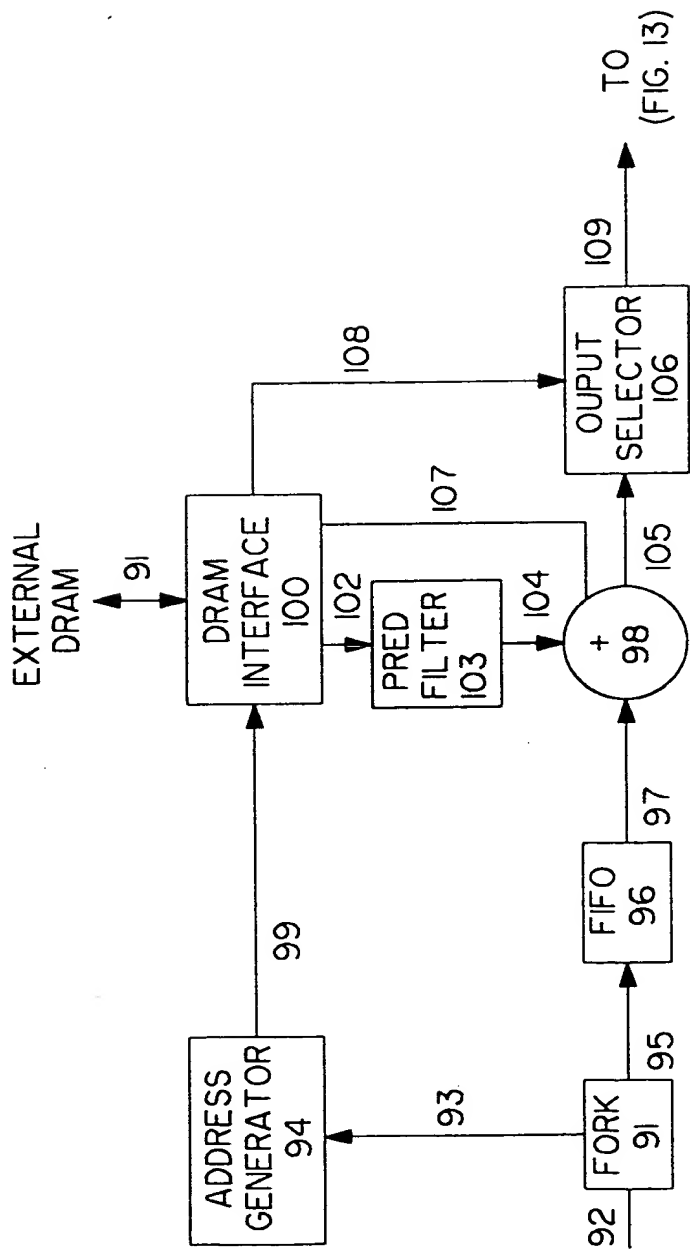


FIG. 12

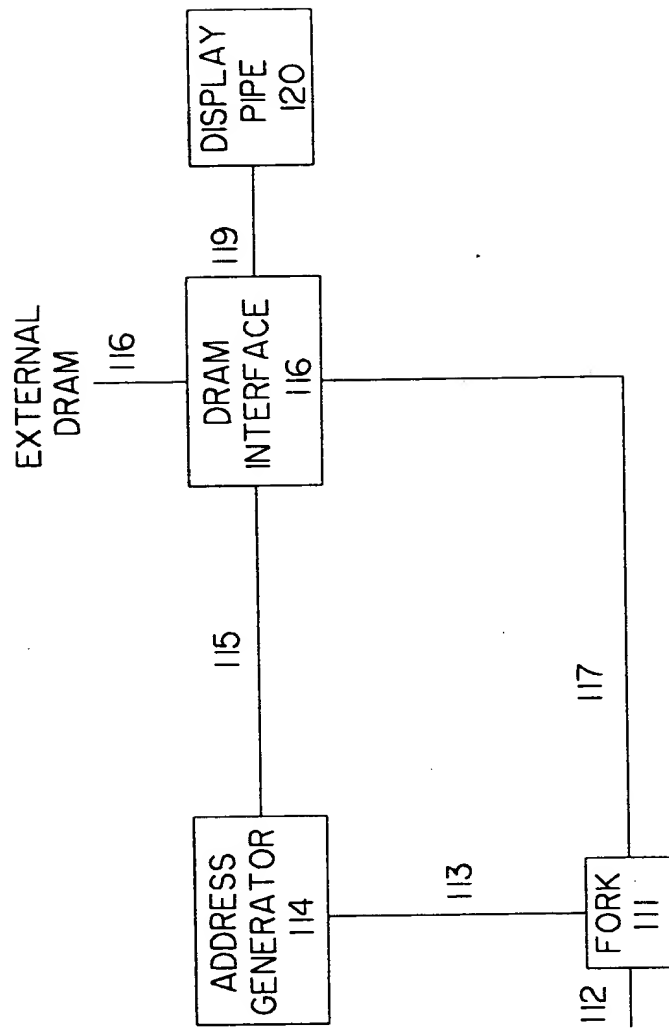
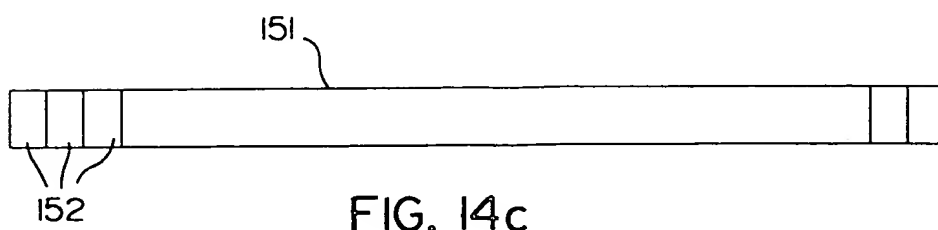
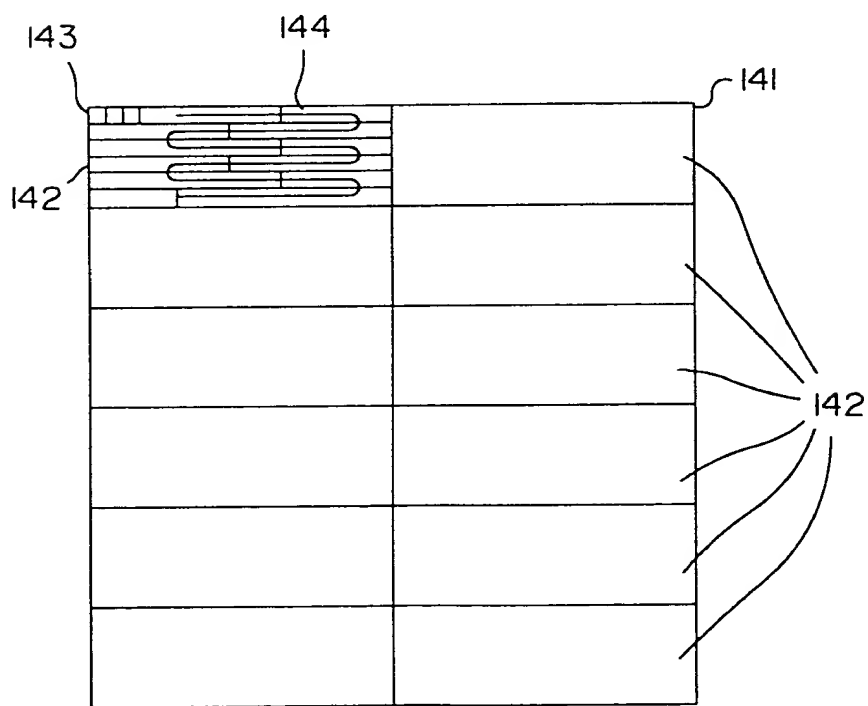
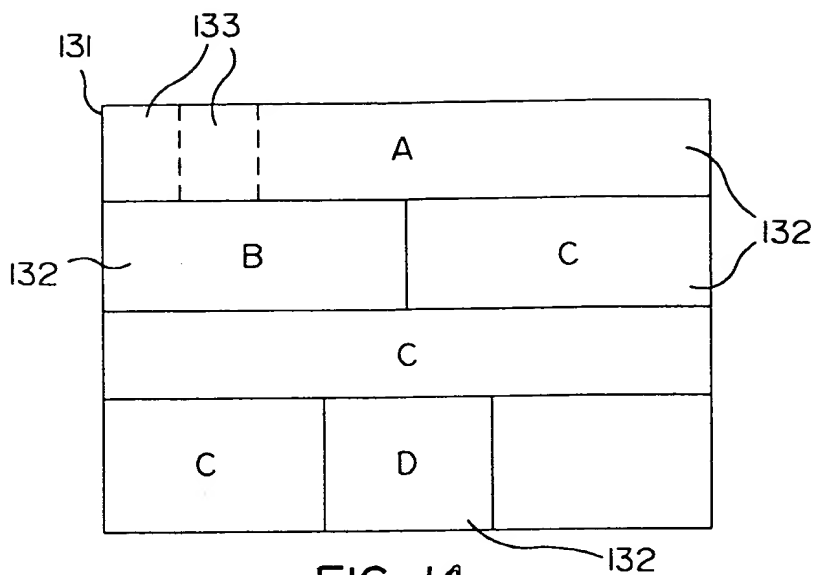


FIG. 13



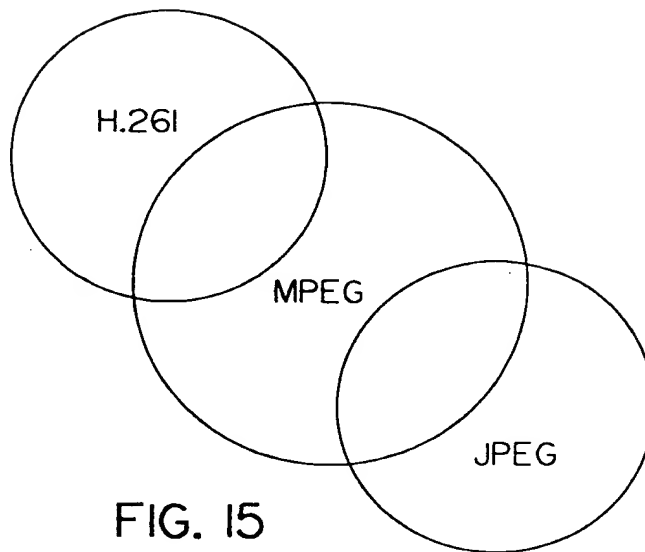


FIG. 15

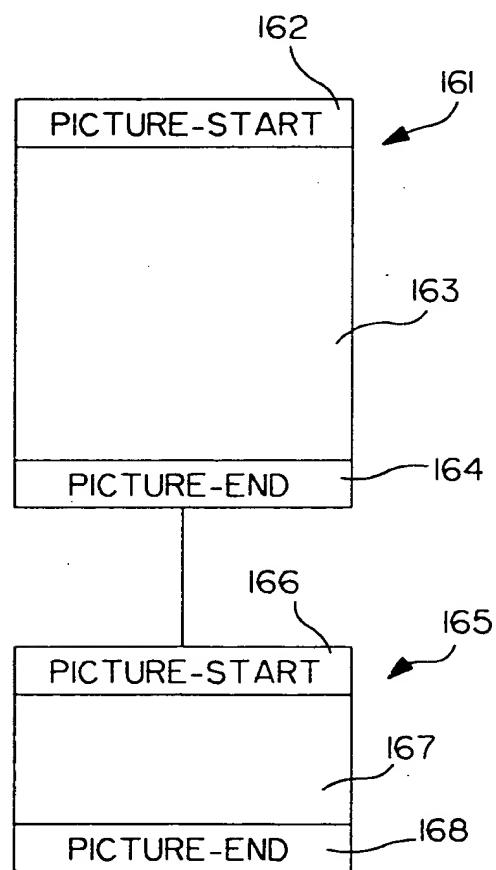
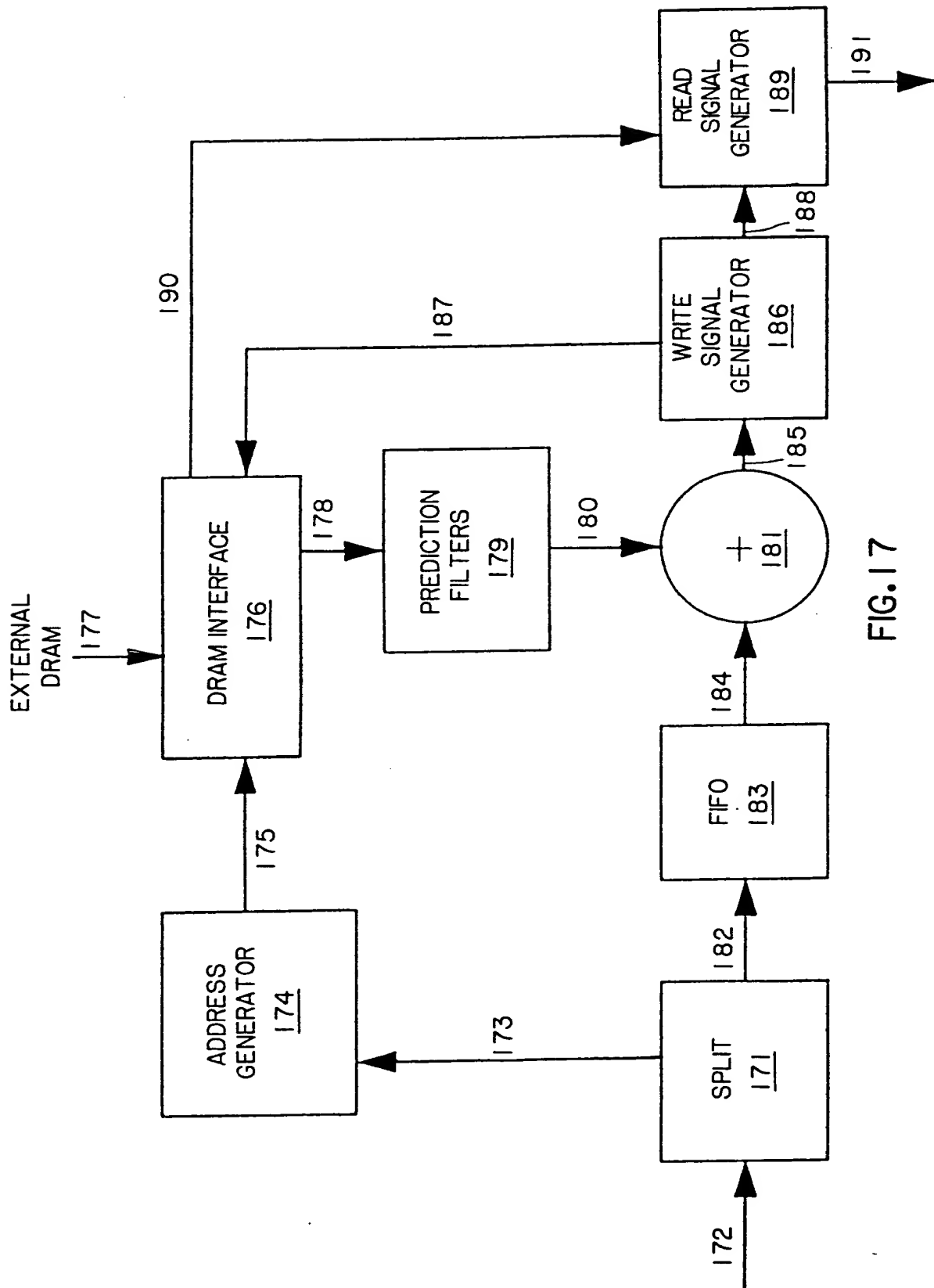


FIG. 16



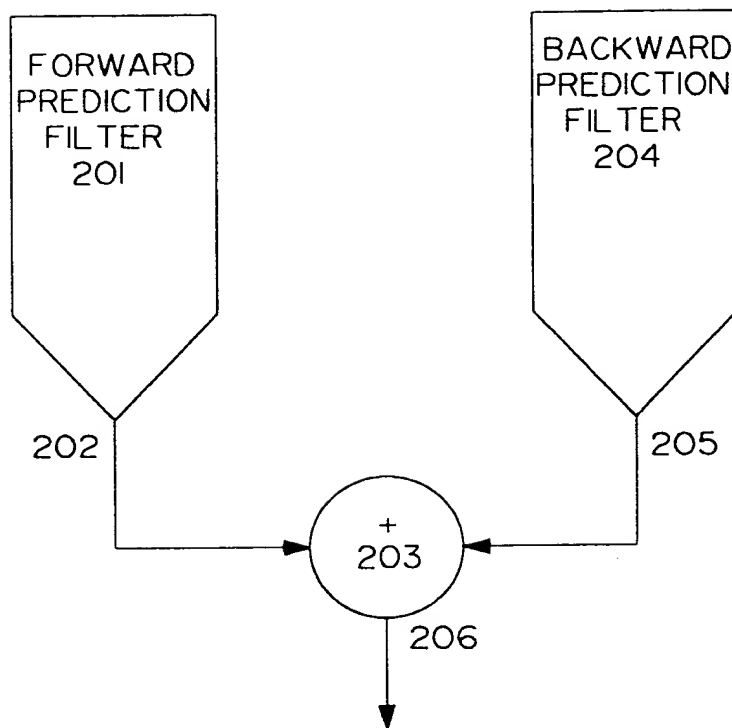


FIG. 18

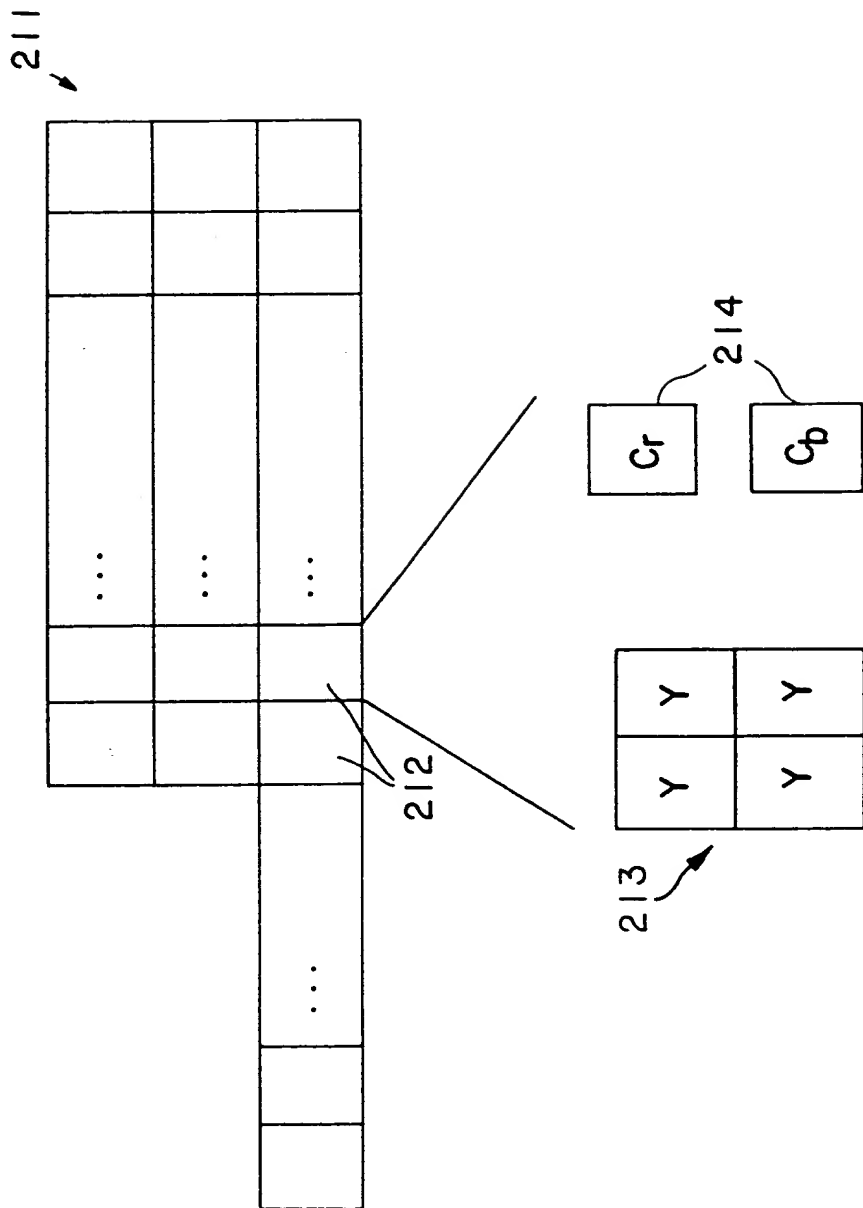


FIG. 19

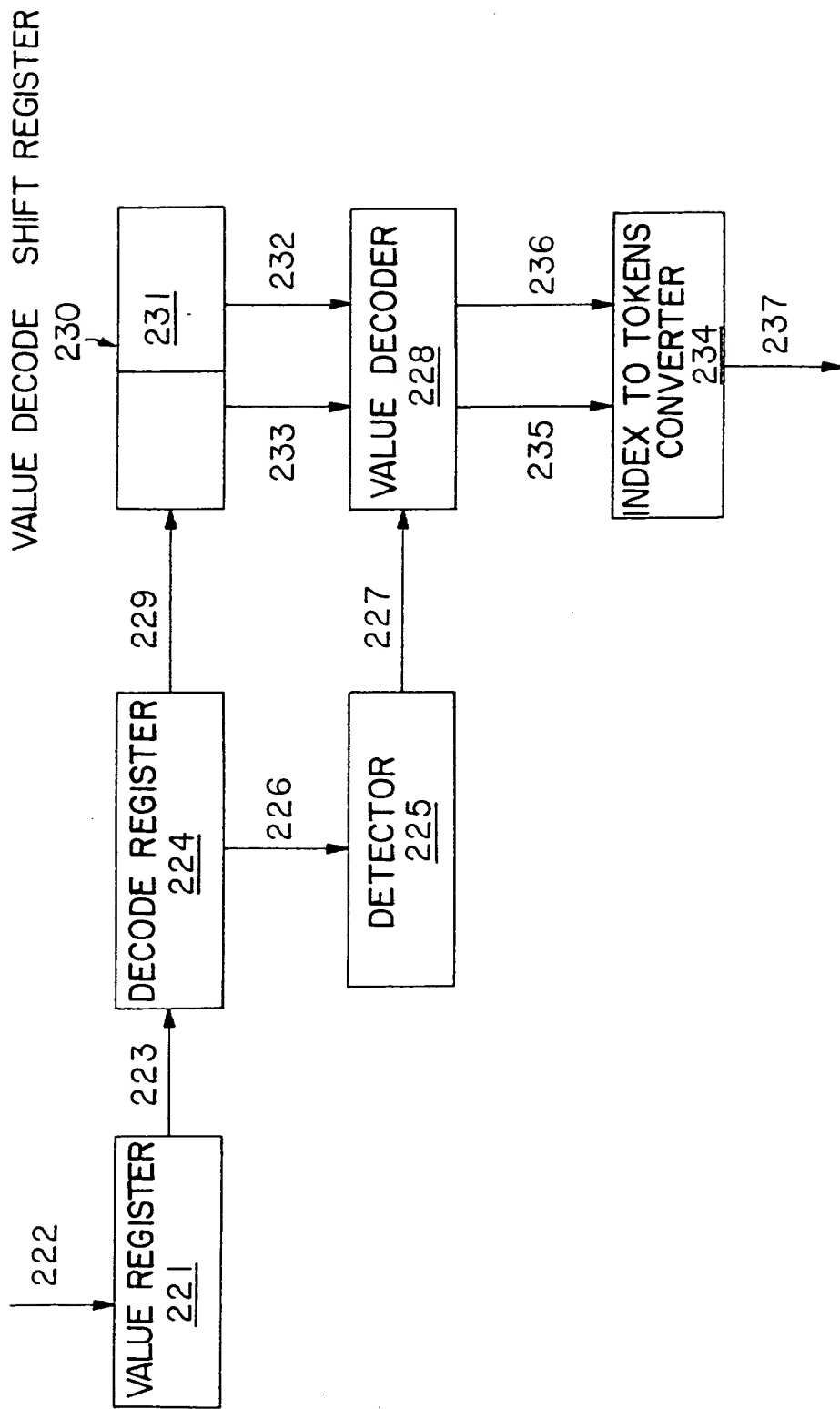


FIG.20

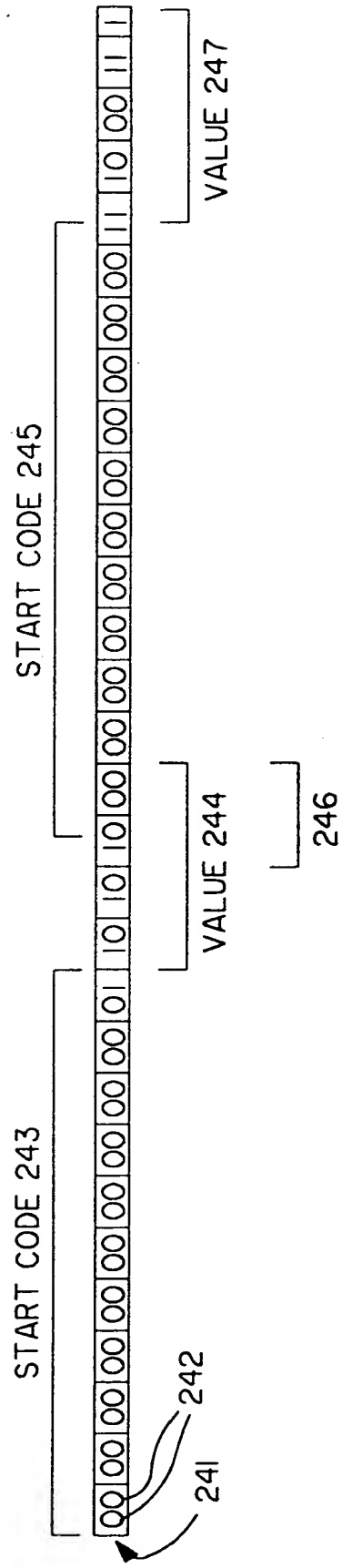


FIG. 21

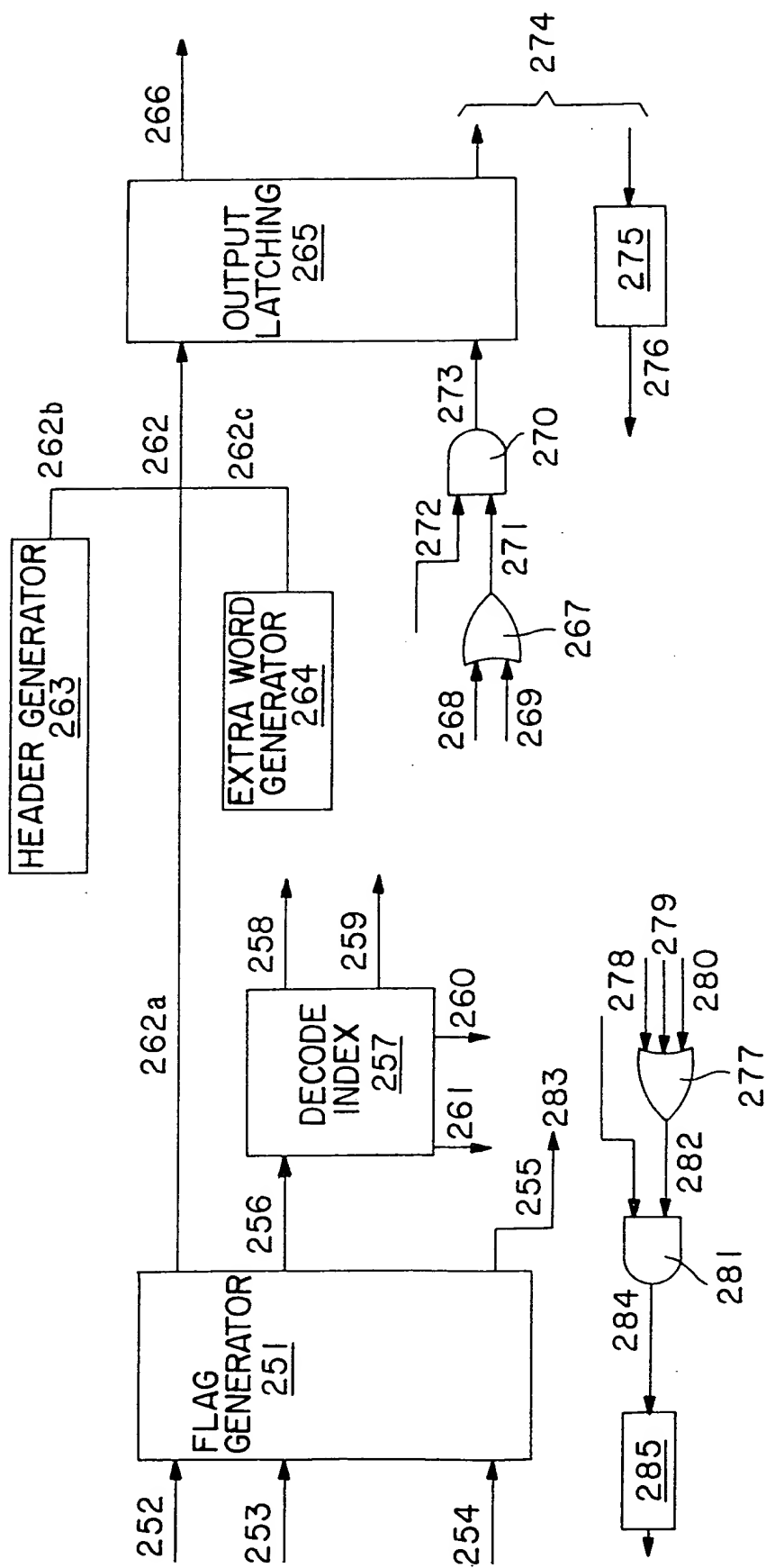


FIG.22

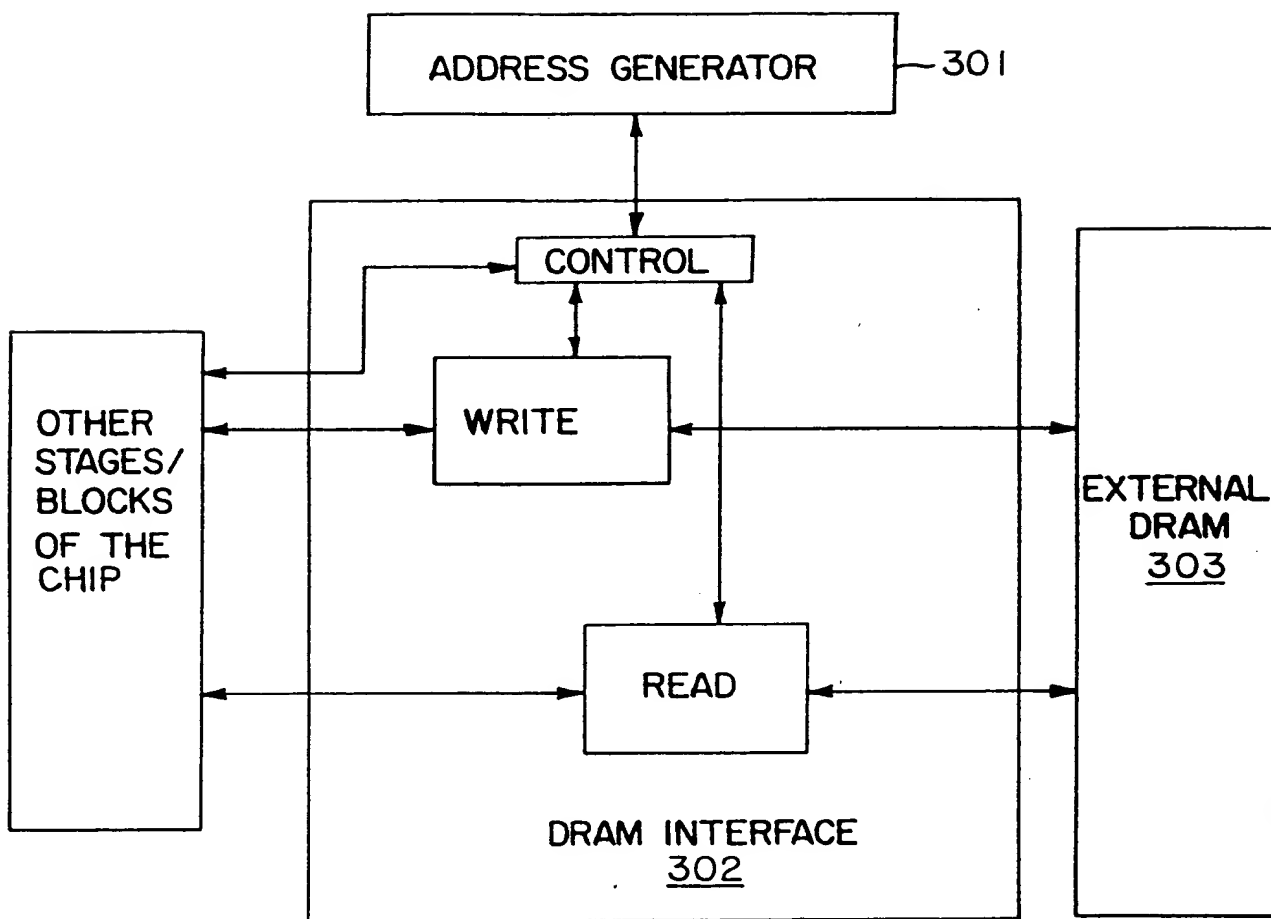


FIG.23

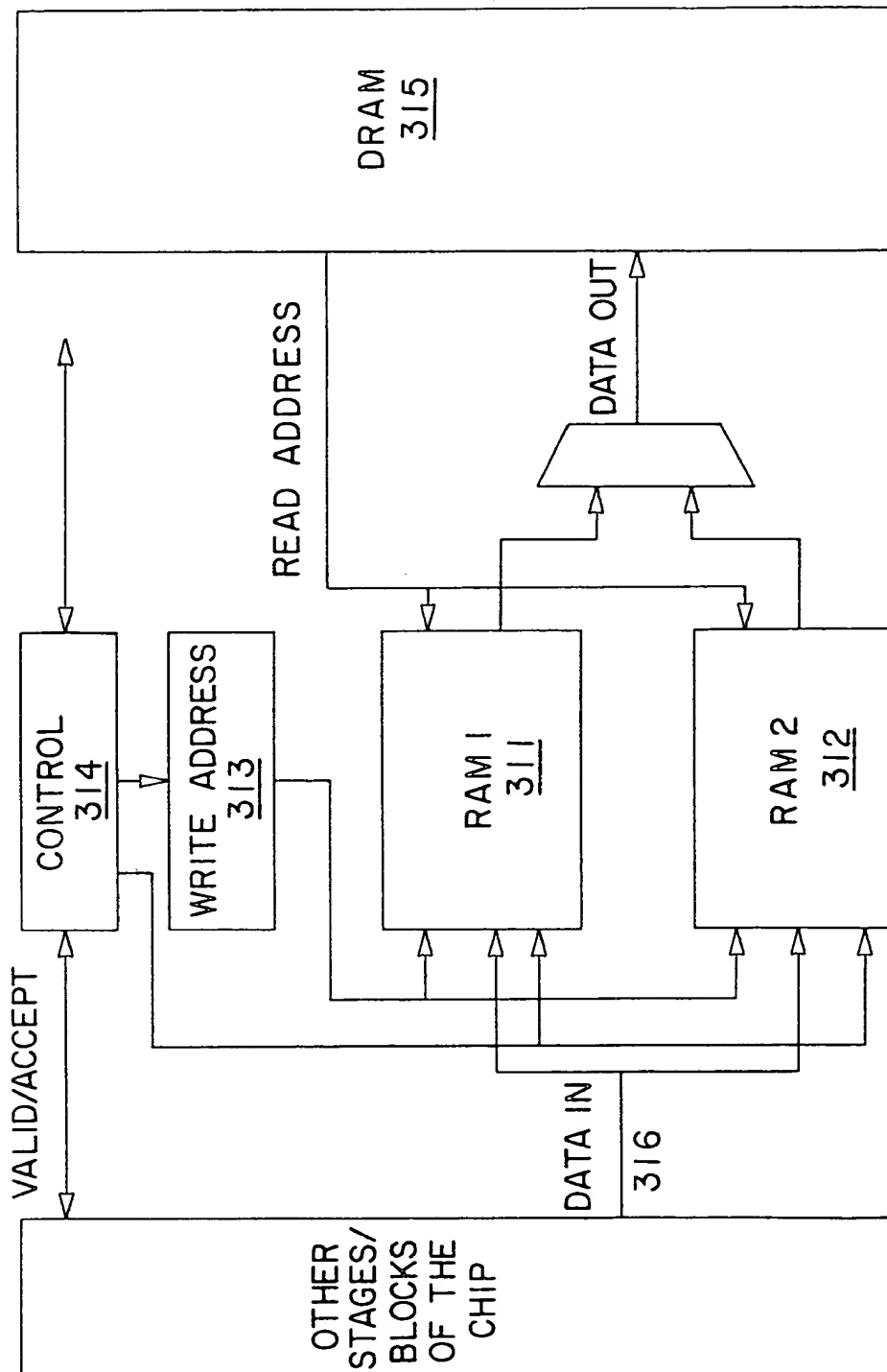


FIG.24

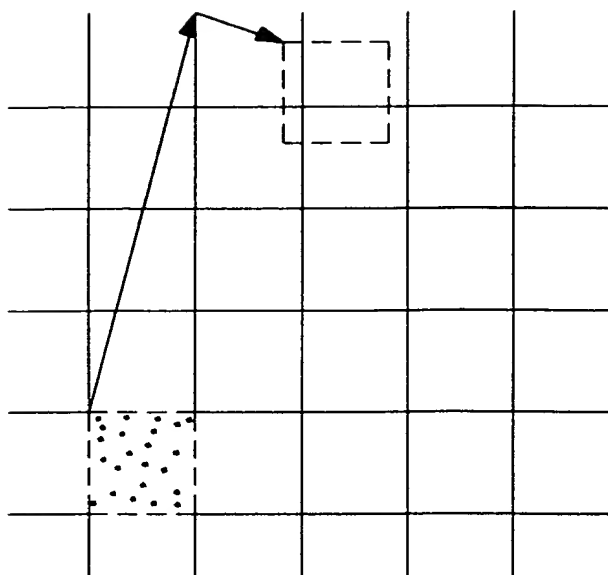


FIG. 25

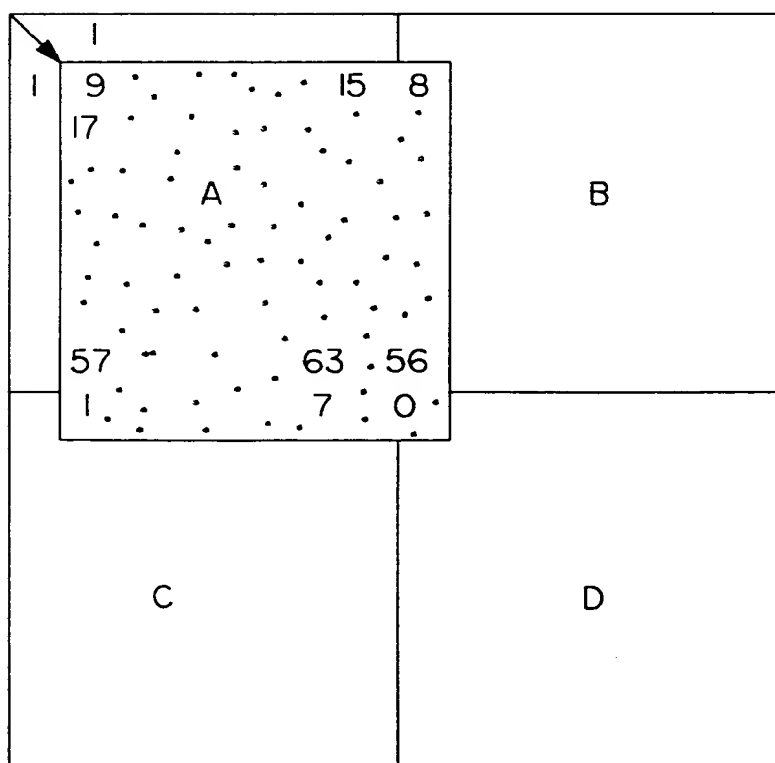


FIG. 26

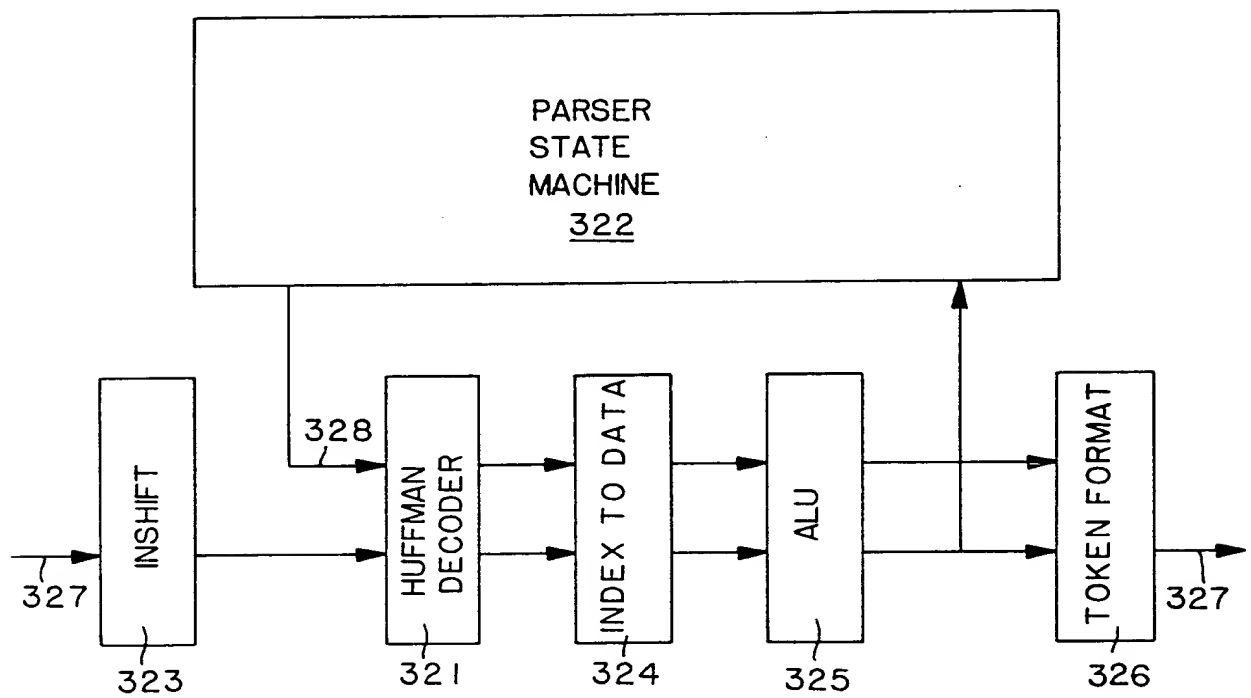


FIG.27

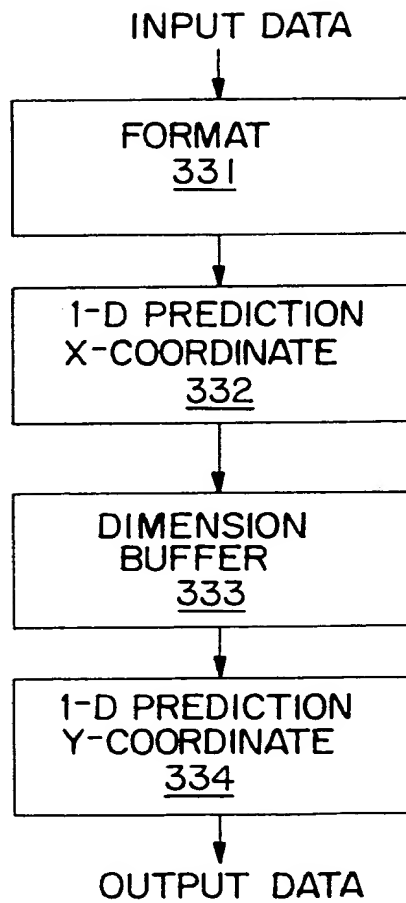


FIG.28

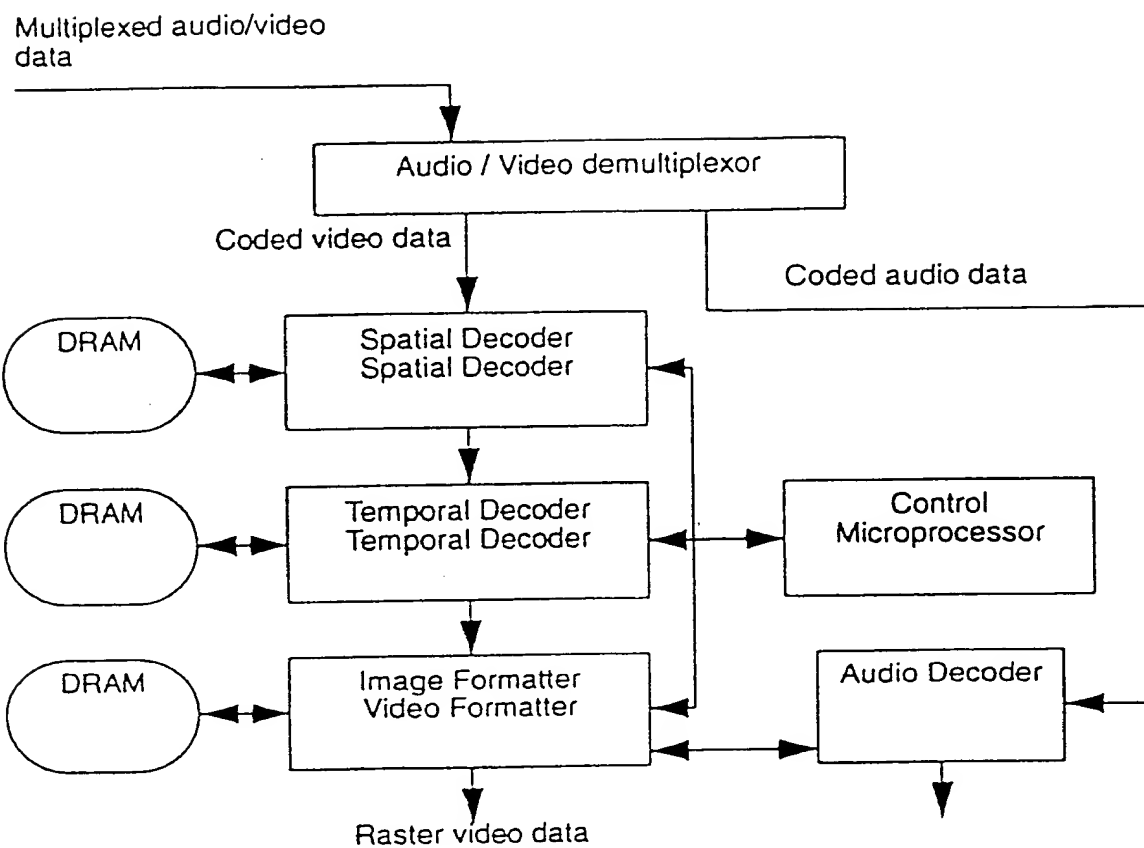


FIG.29

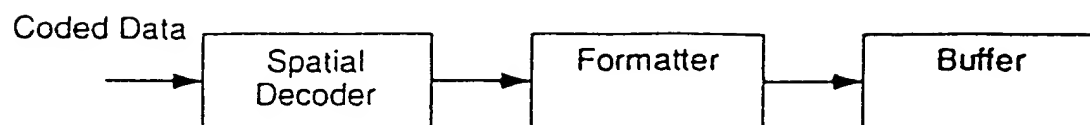


FIG.30

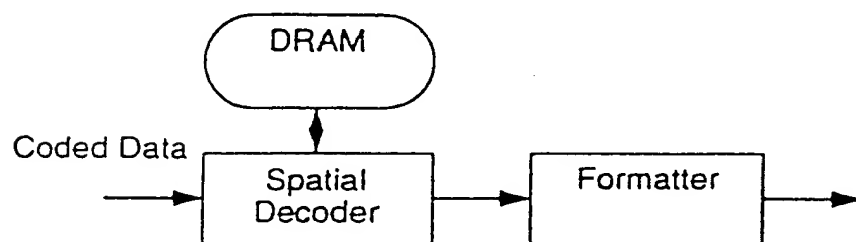


FIG.31

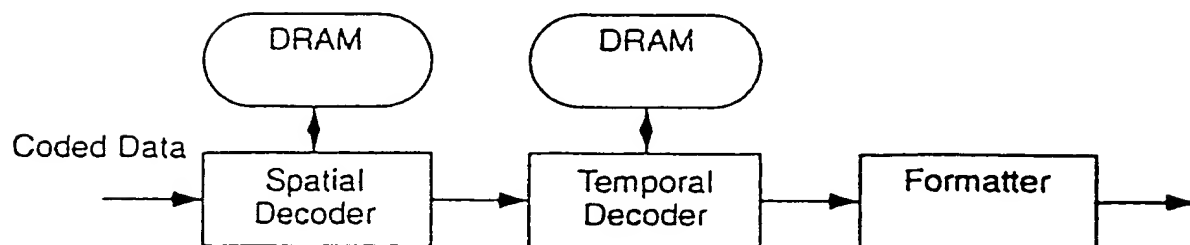


FIG.32

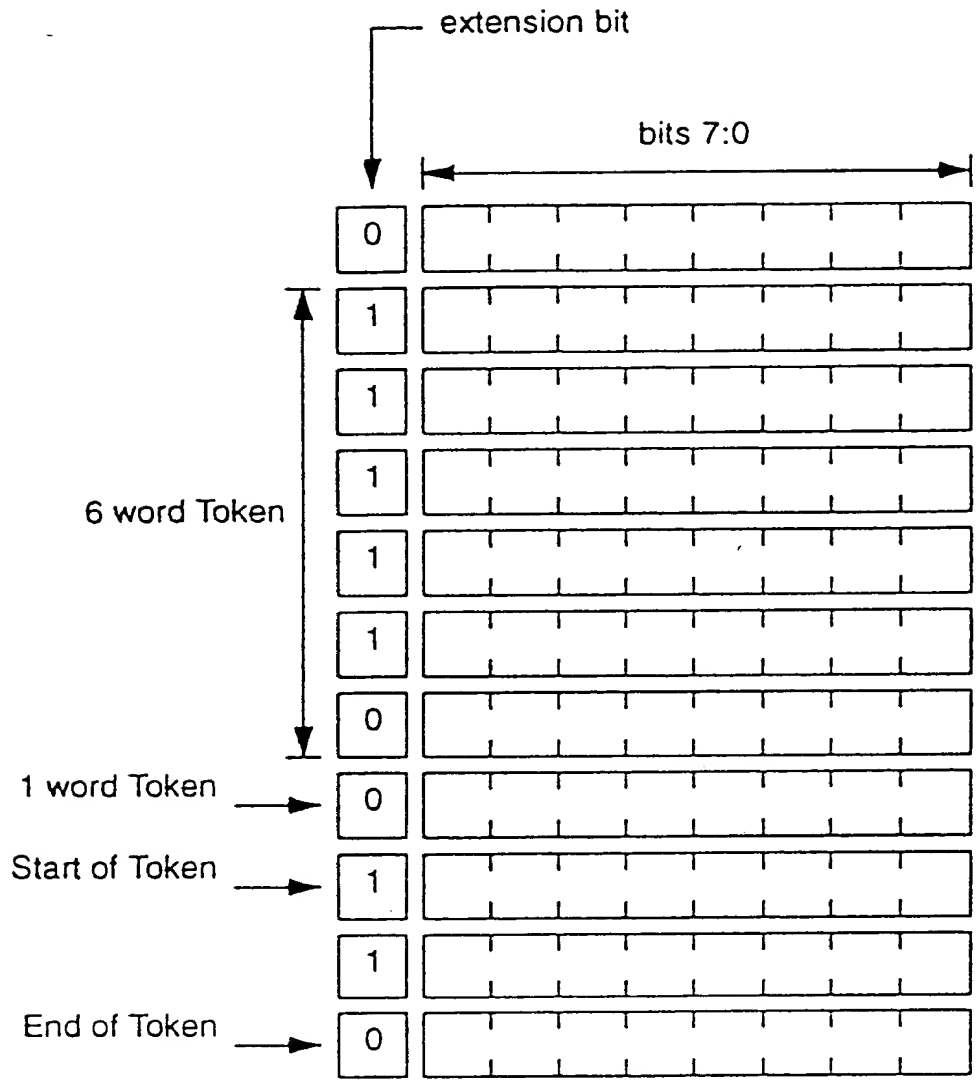


FIG.33

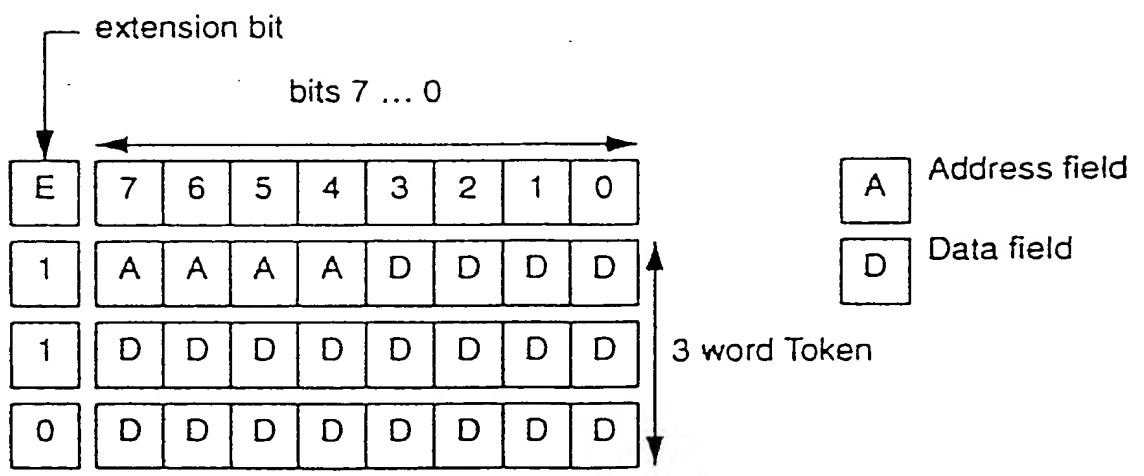


FIG.34

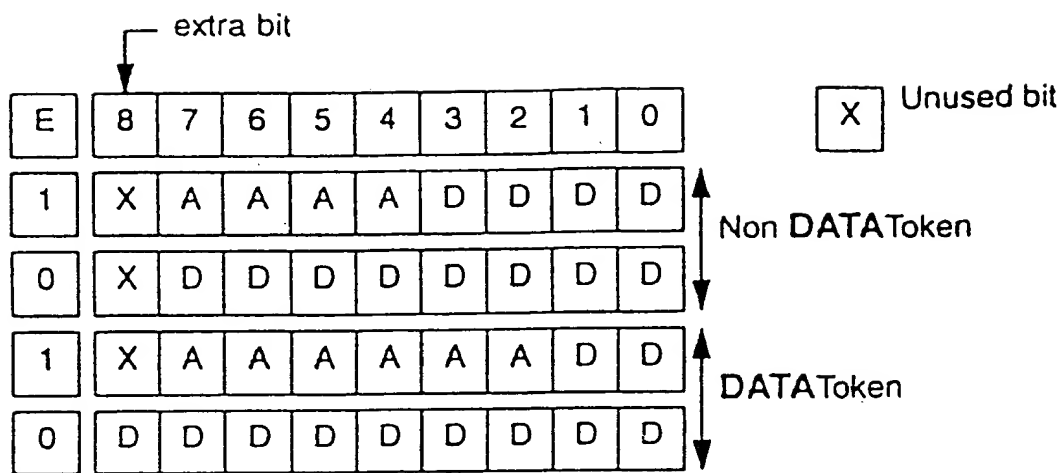
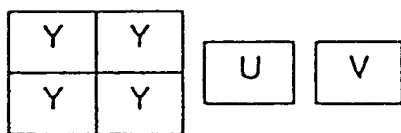


FIG.35



MPEG 4:2:0
macroblock

FIG.36A



JPEG 2:1:1
macroblock

FIG.36B

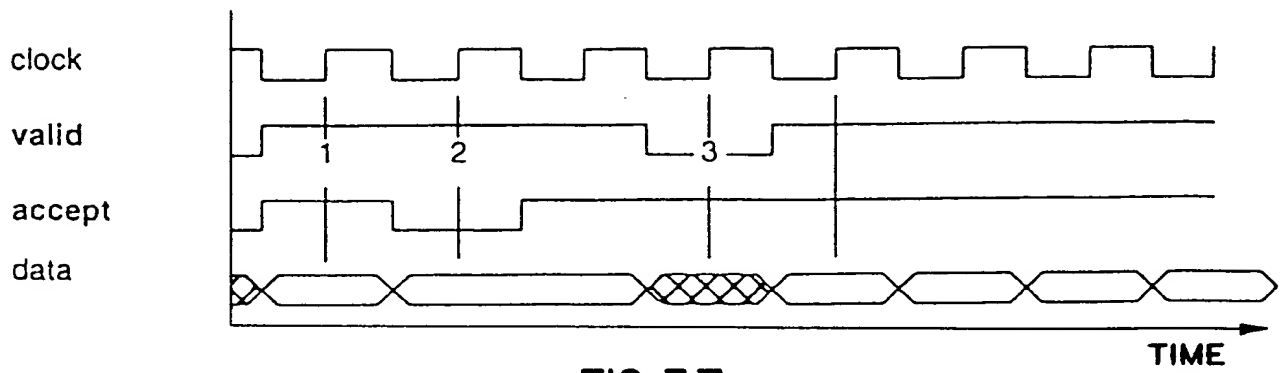


FIG.37

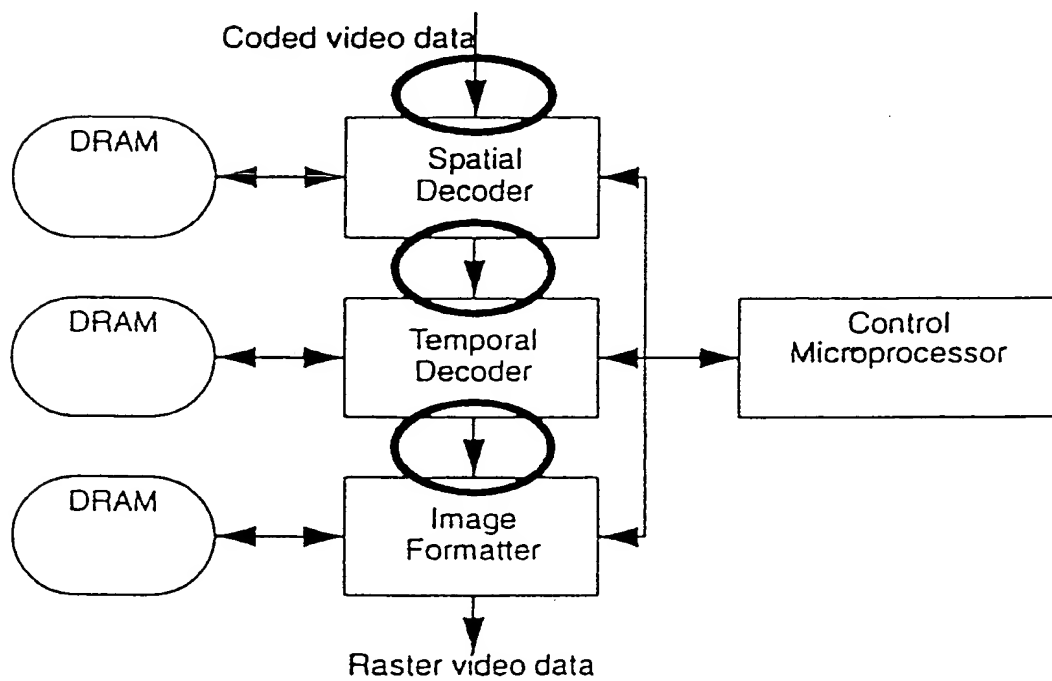


FIG.38

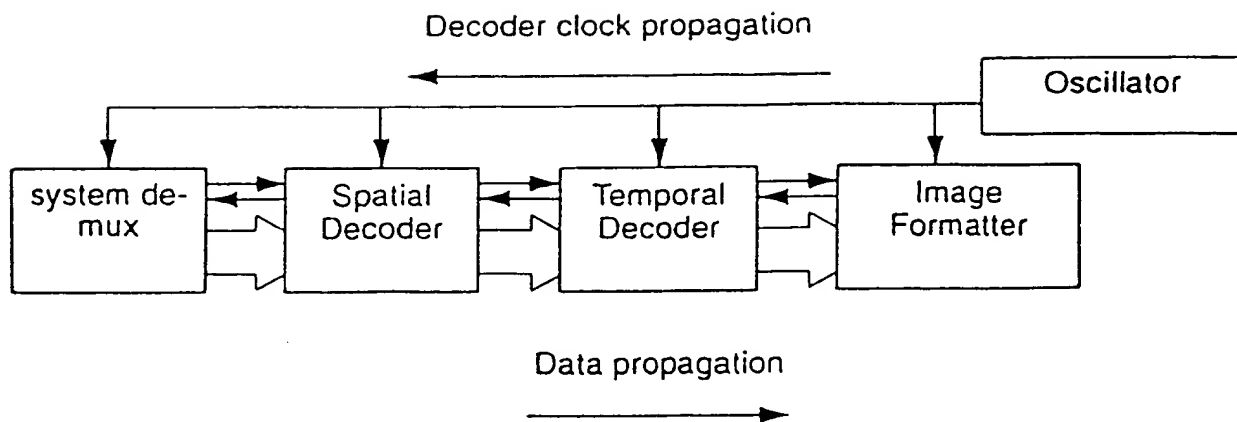


FIG.39

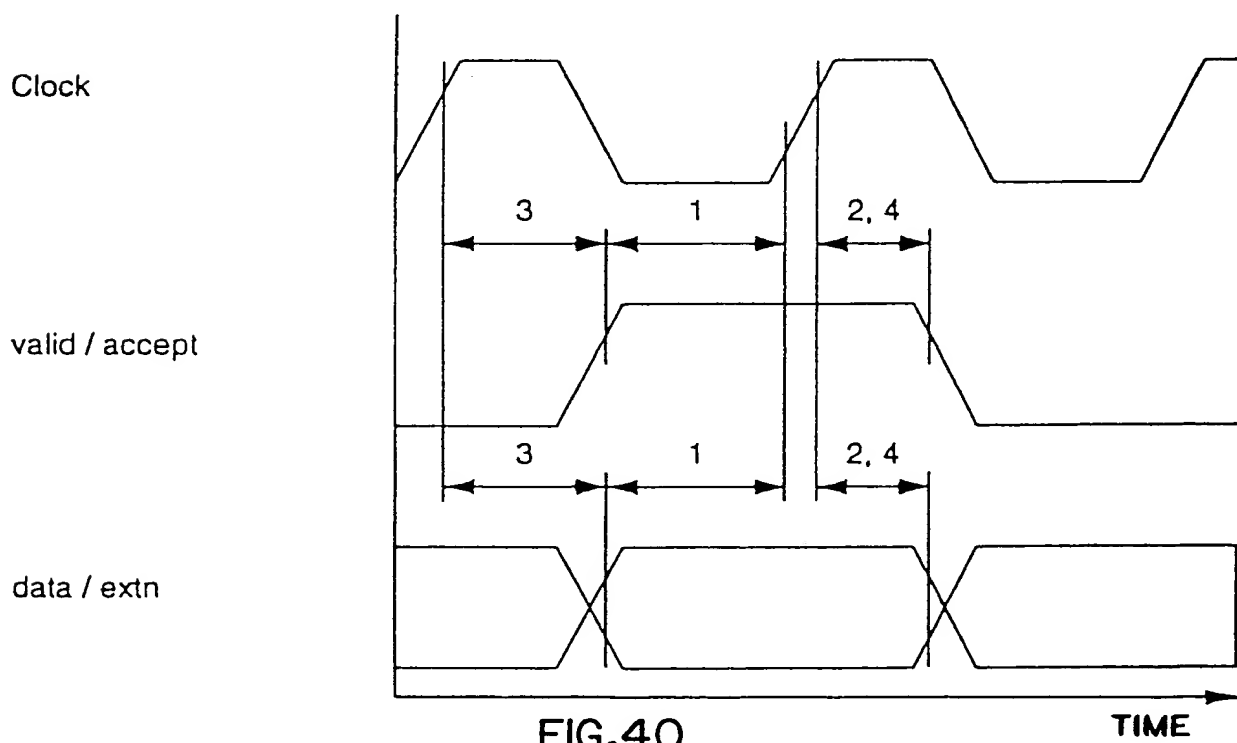


FIG.40



FIG.41

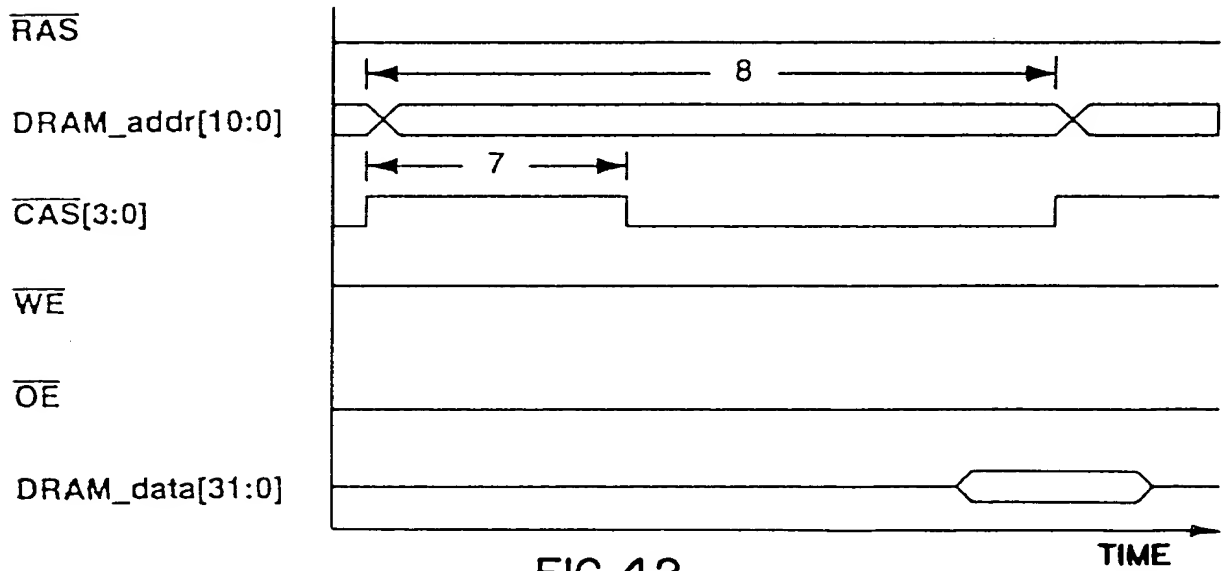


FIG.42

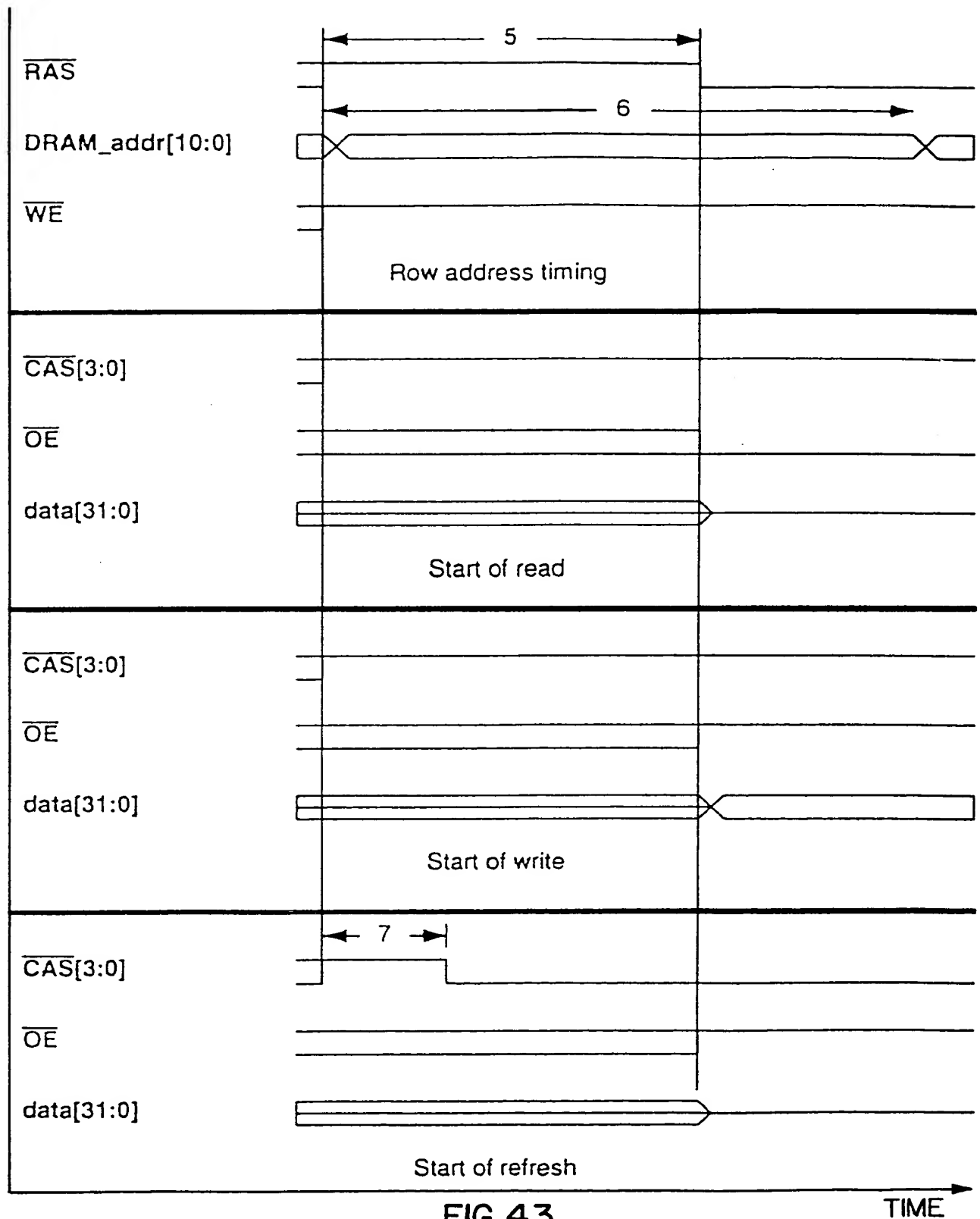


FIG.43

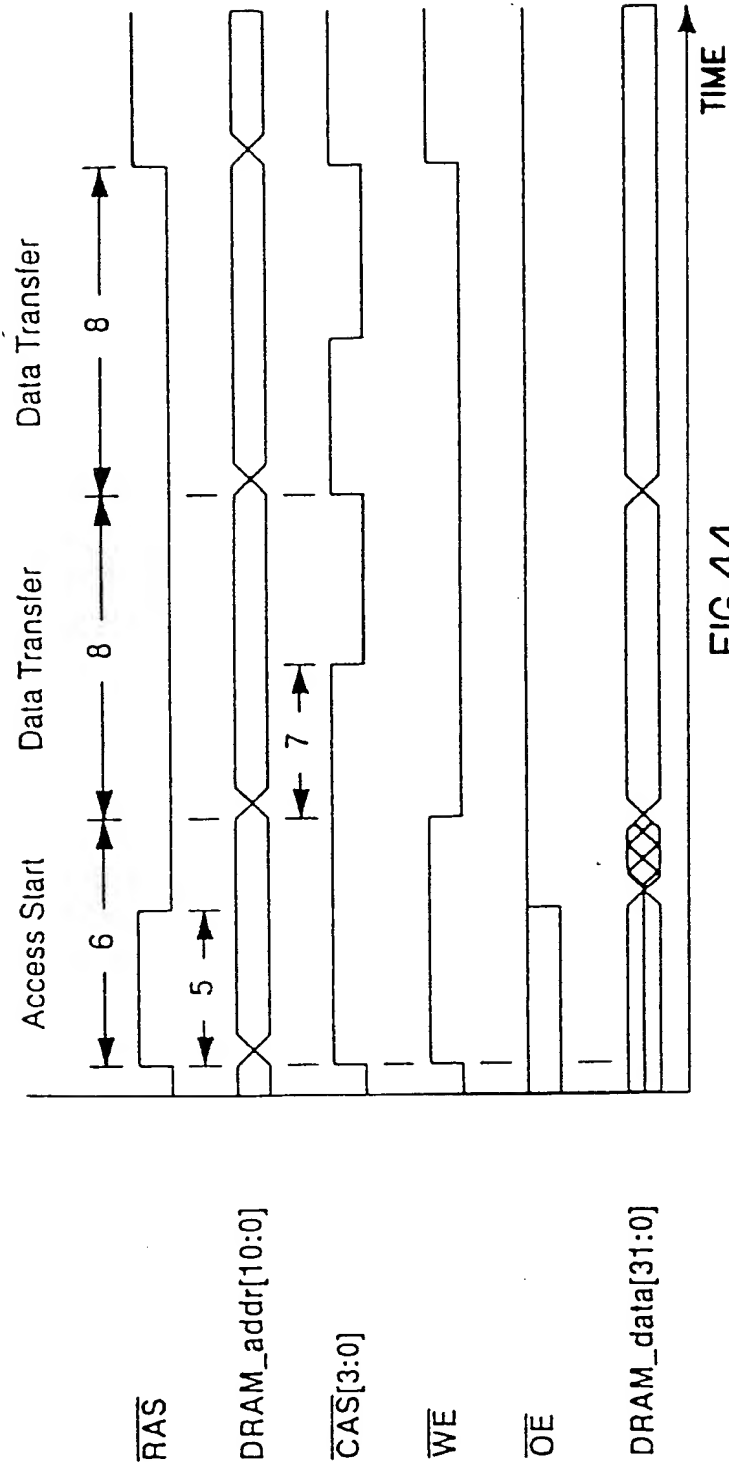


FIG.44

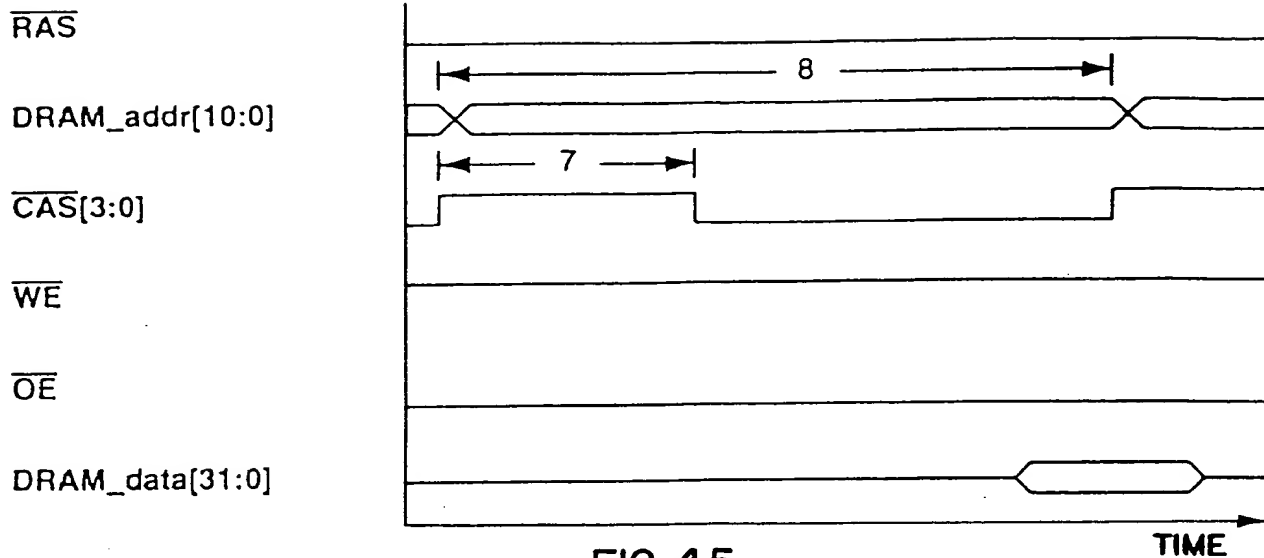


FIG. 45

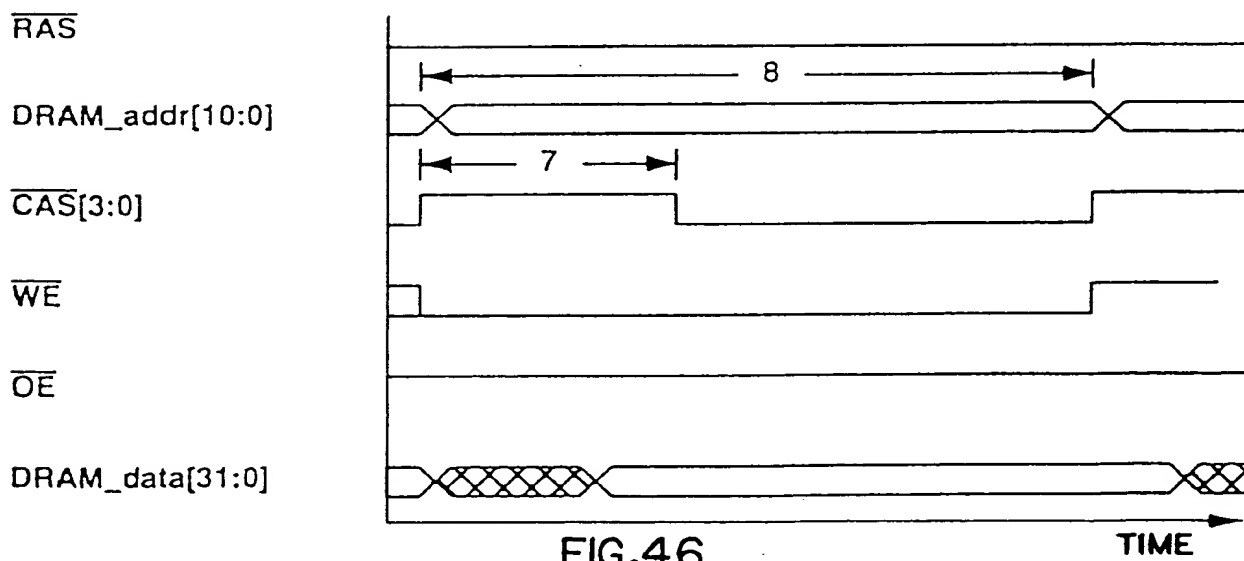


FIG. 46

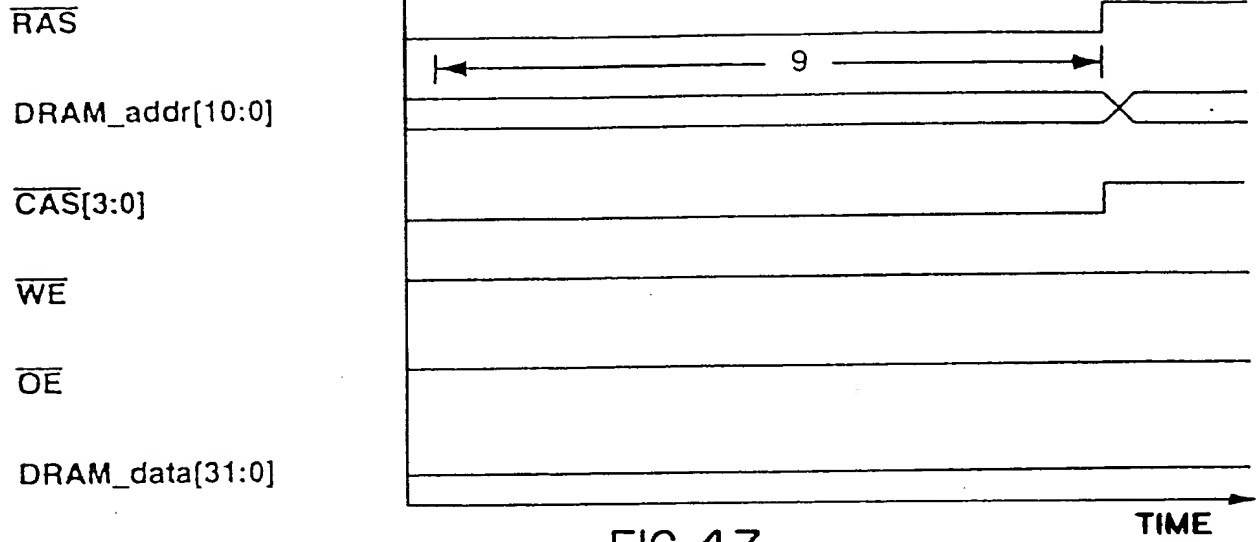


FIG.47

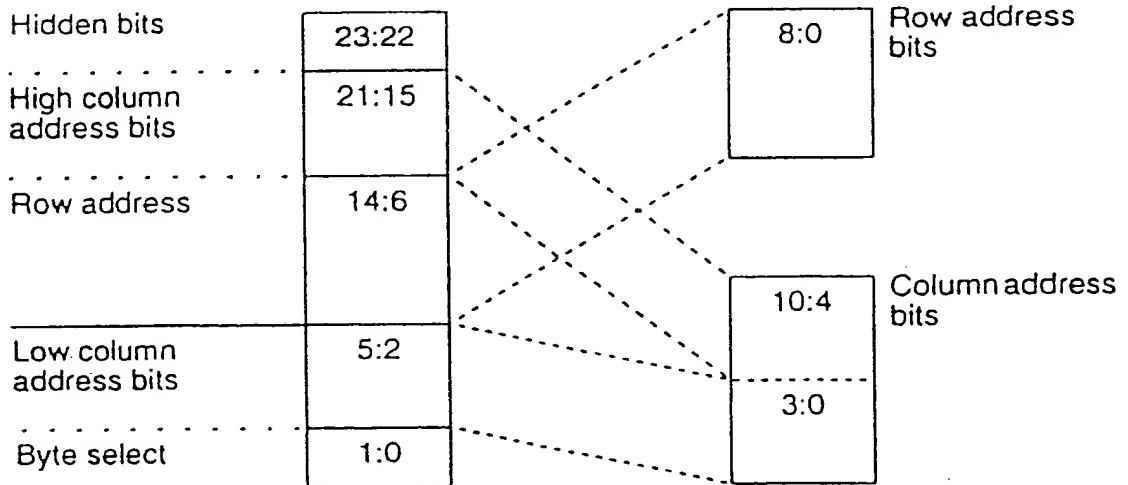


FIG.48

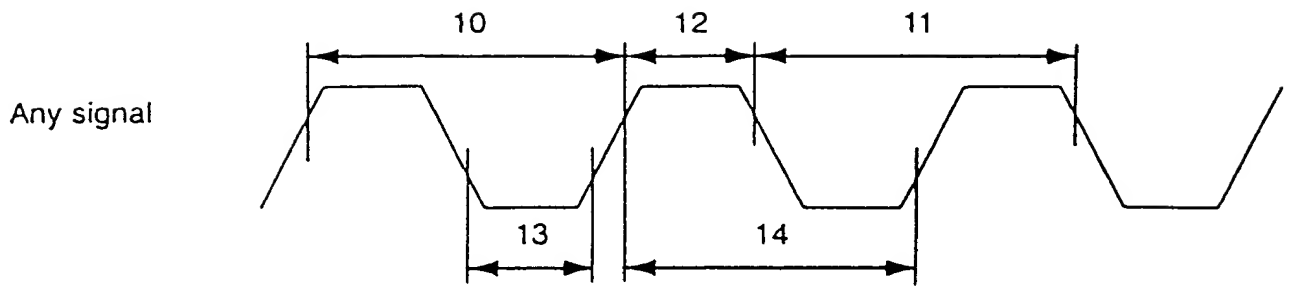


FIG. 49

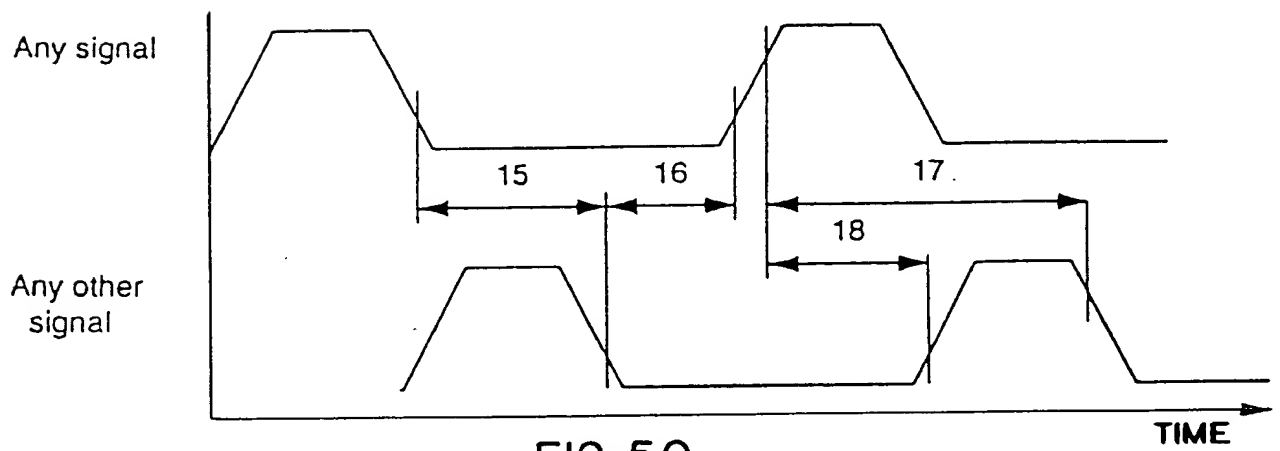


FIG. 50

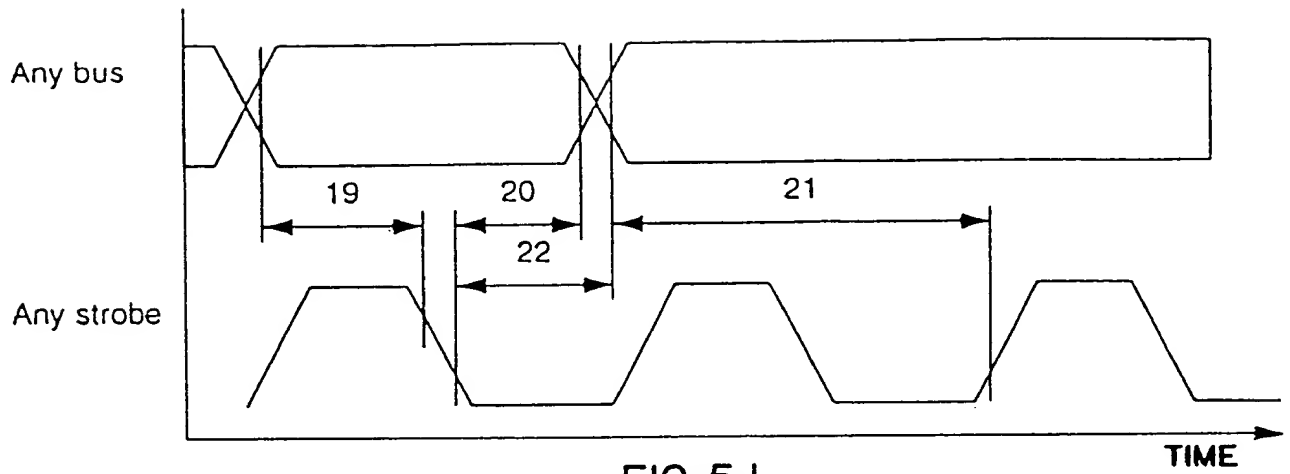


FIG.51

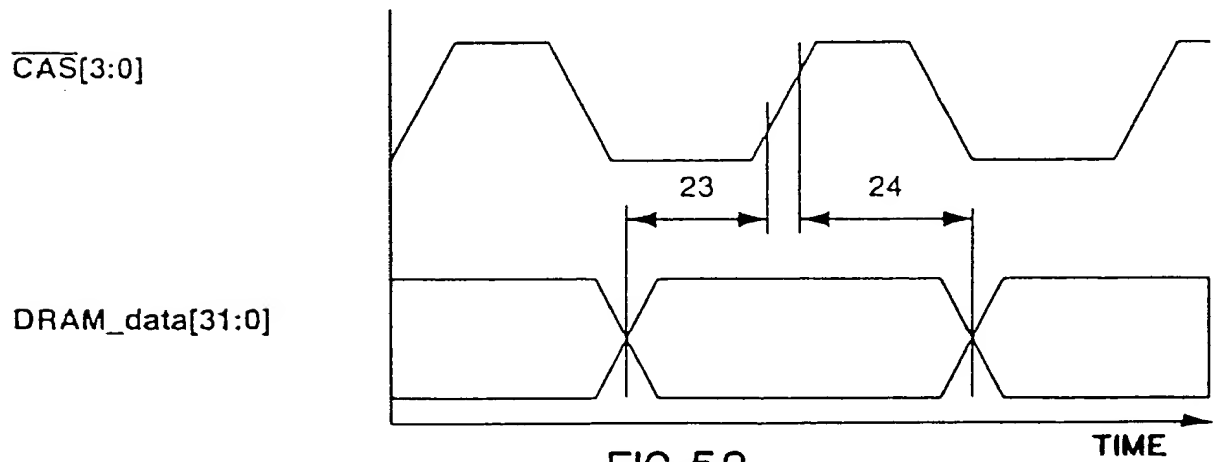
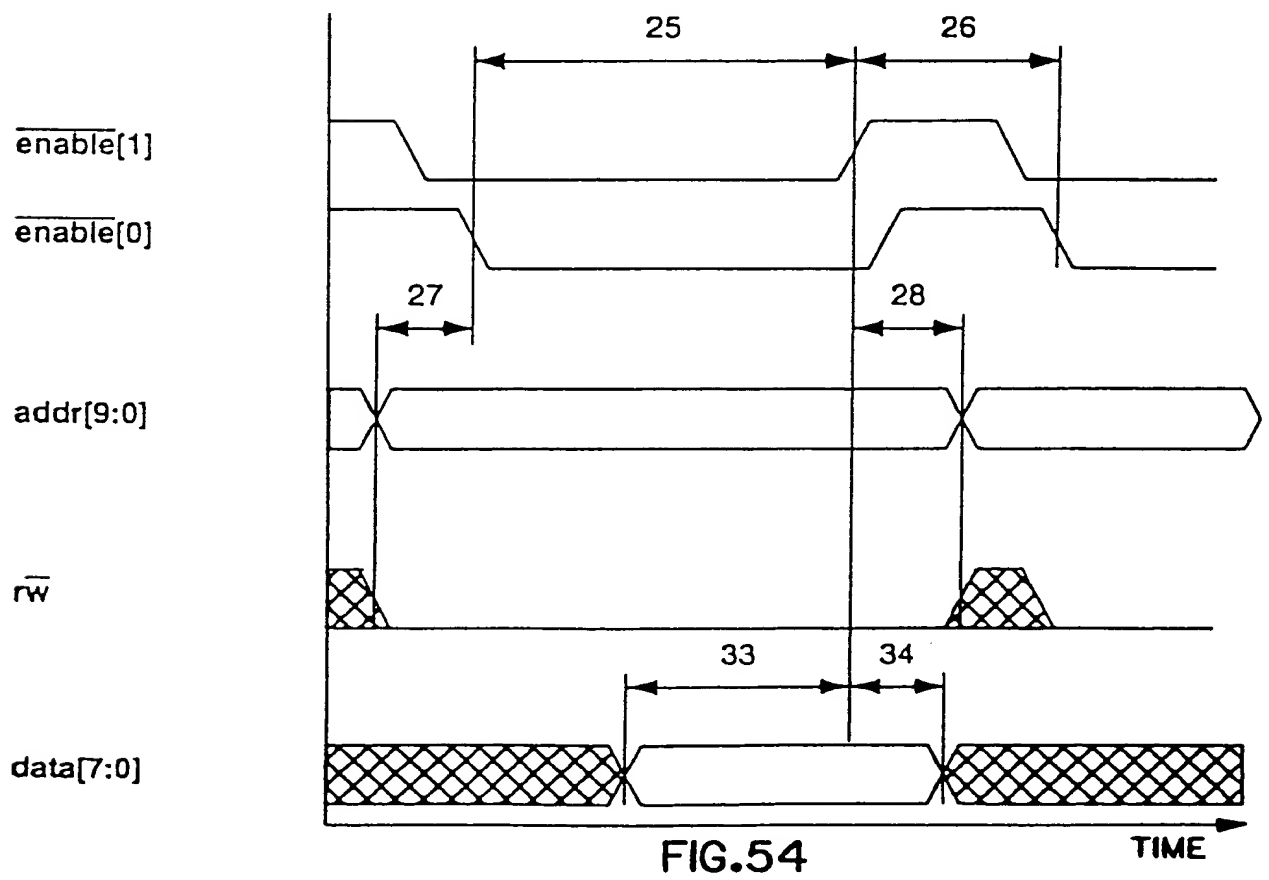
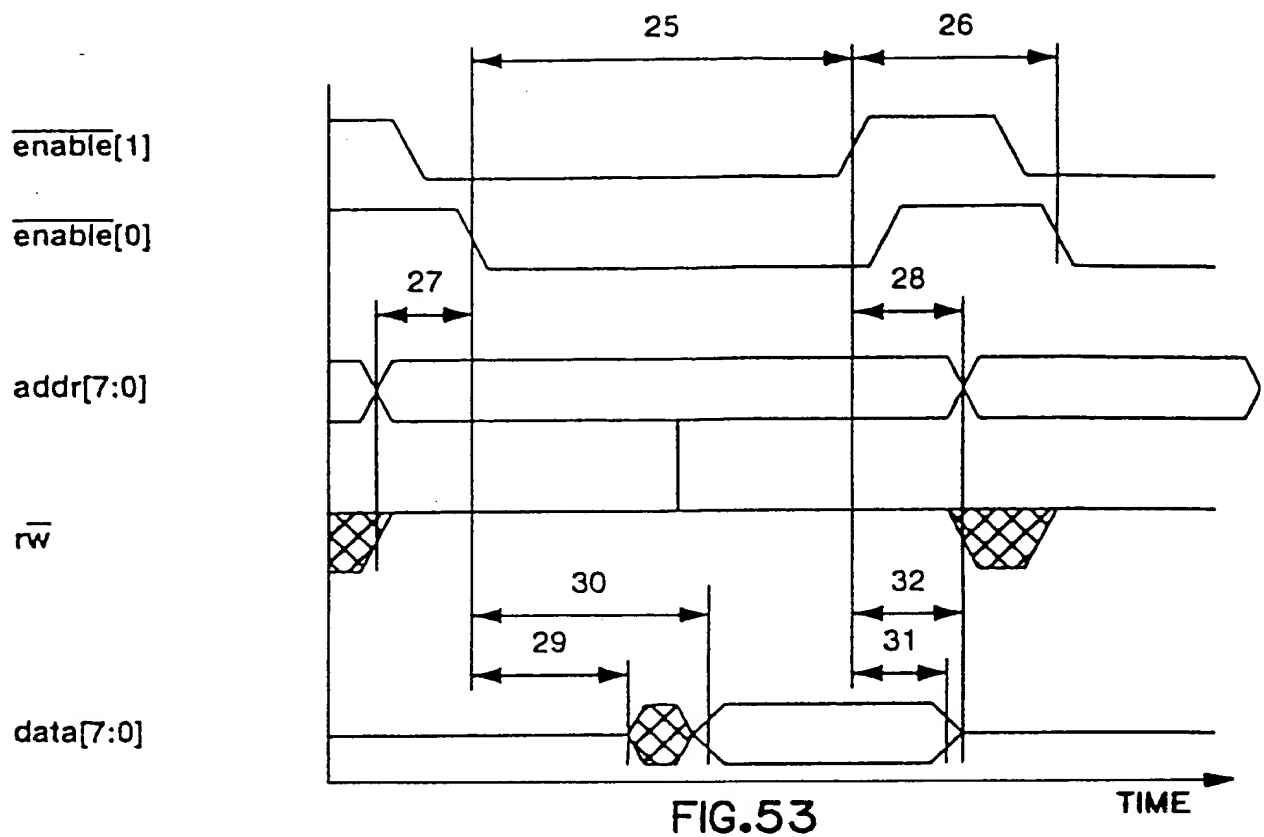


FIG.52



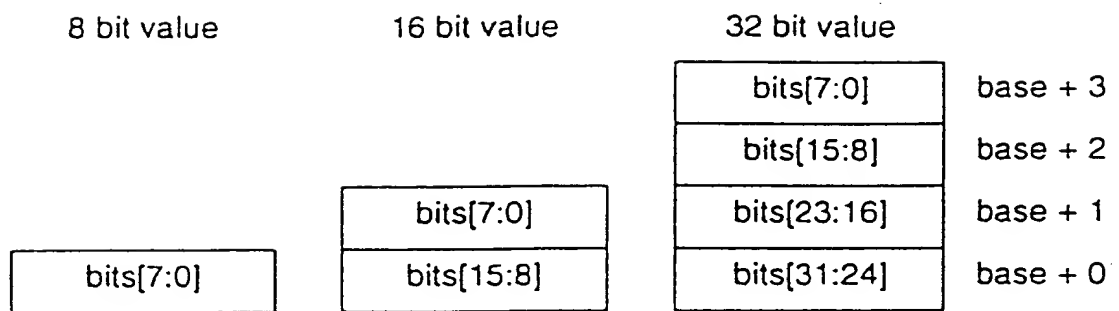


FIG.55

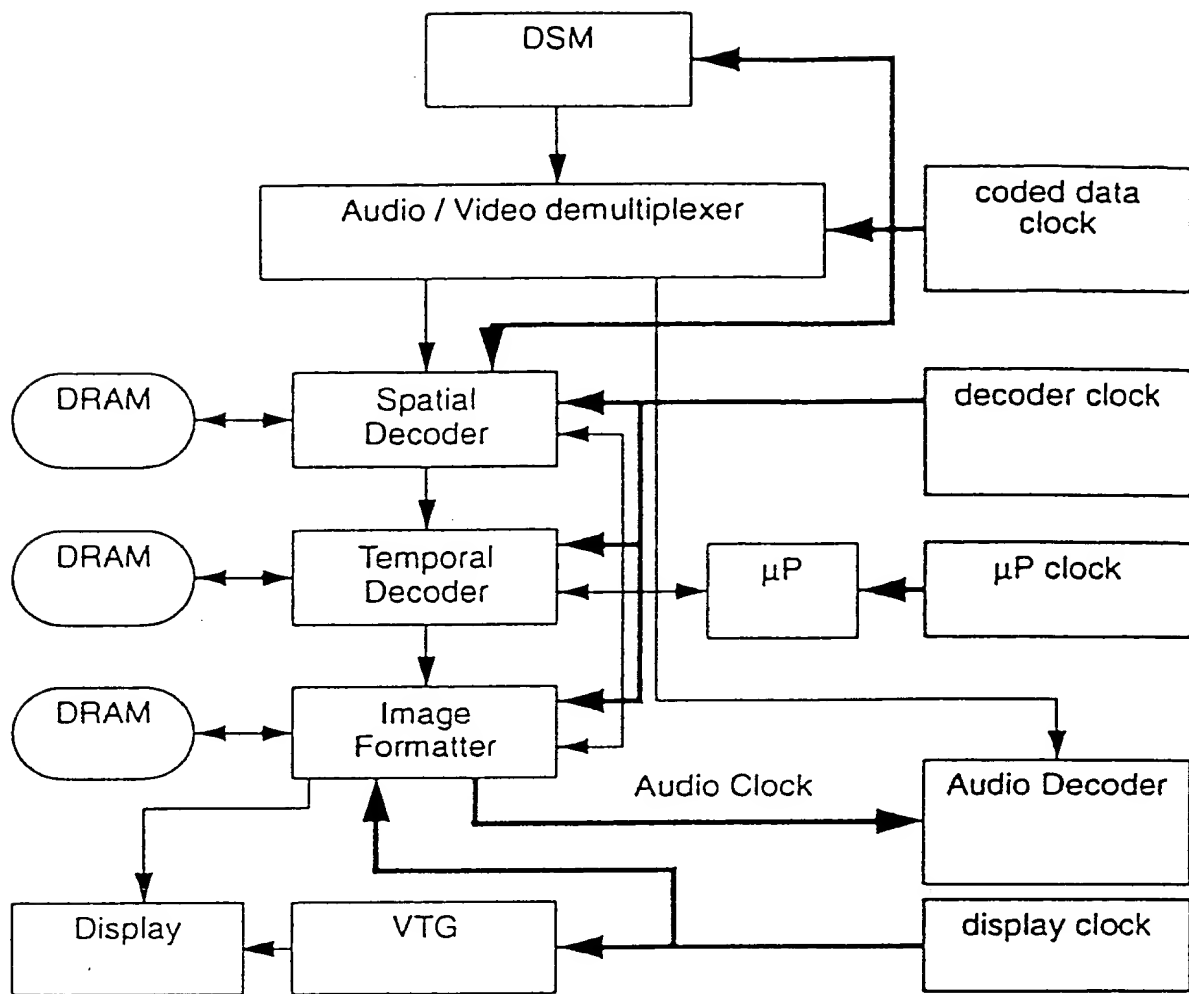


FIG.56

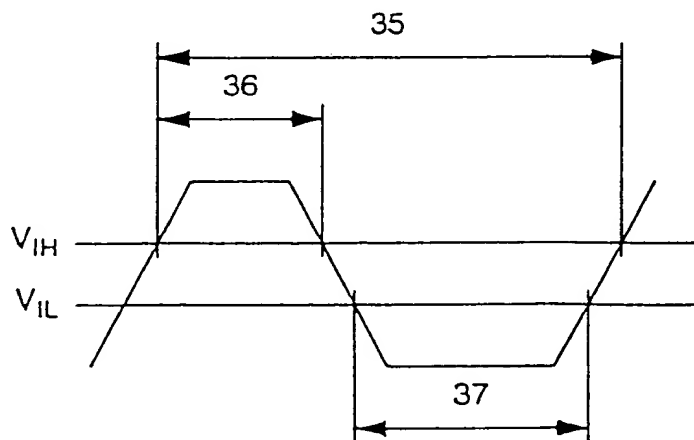


FIG.57

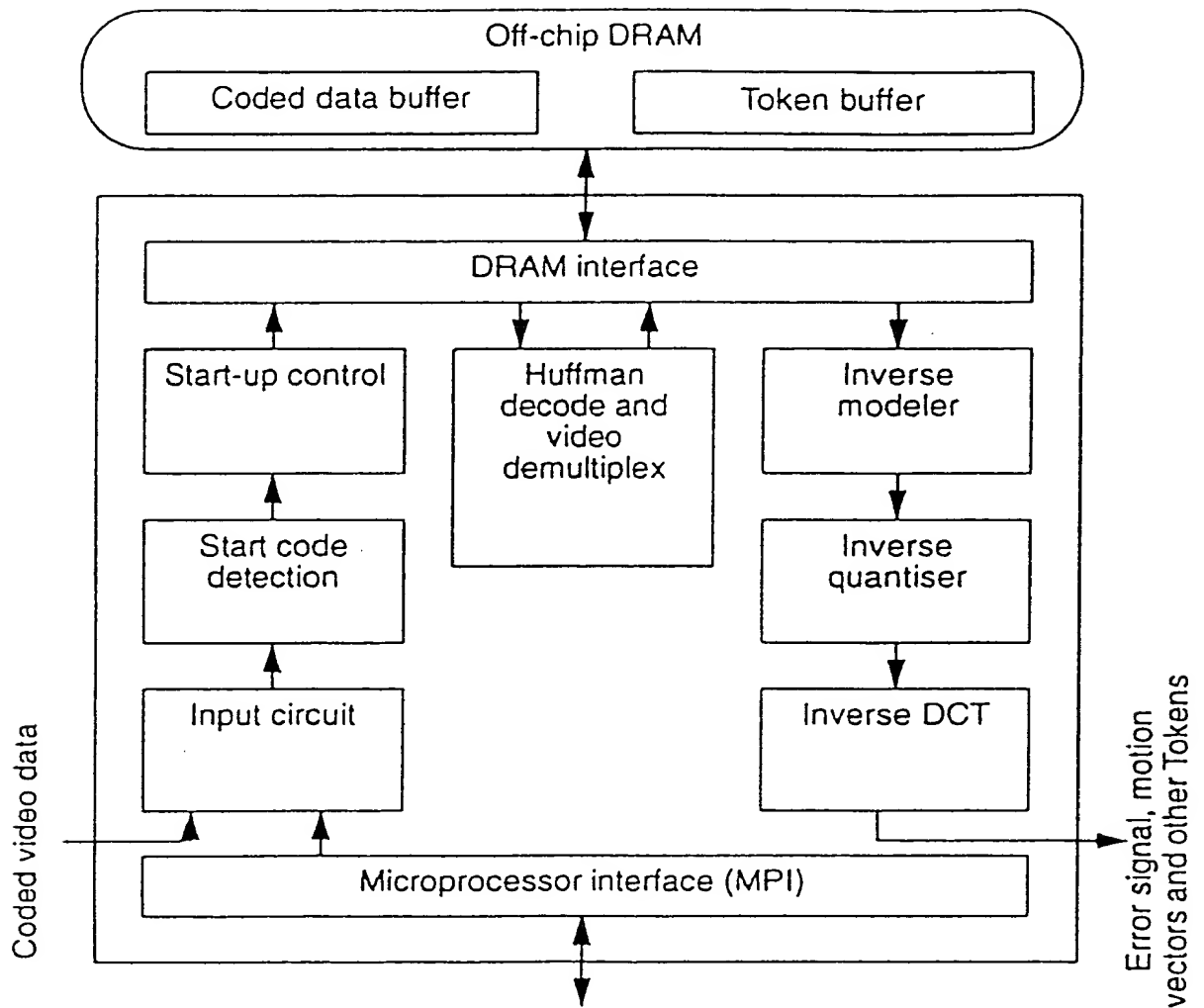


FIG.58

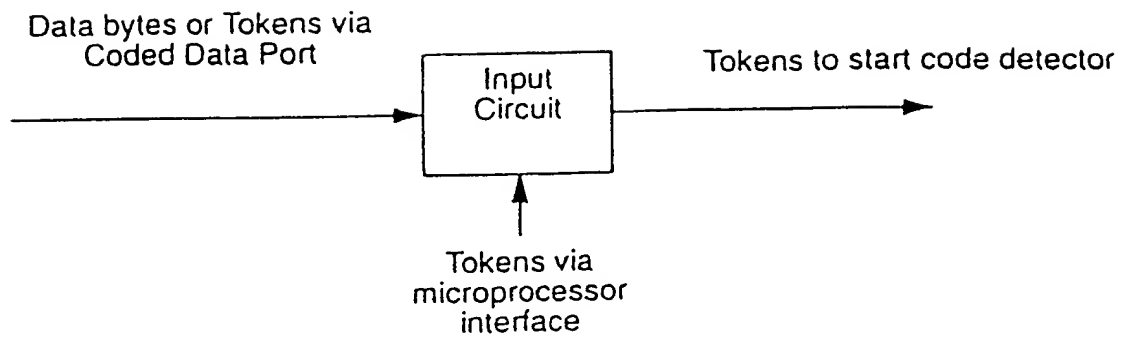


FIG.59

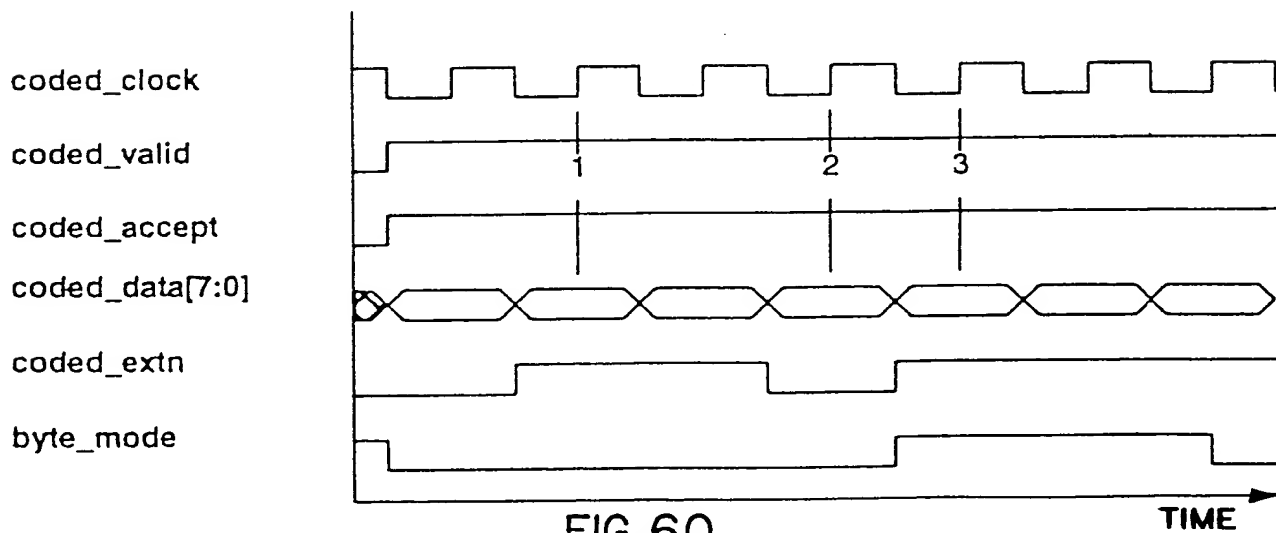


FIG.60

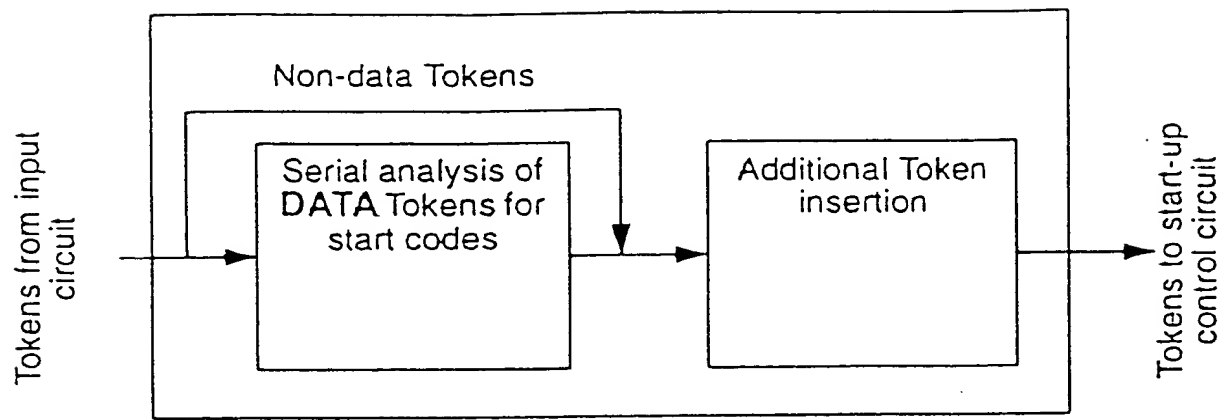


FIG.61

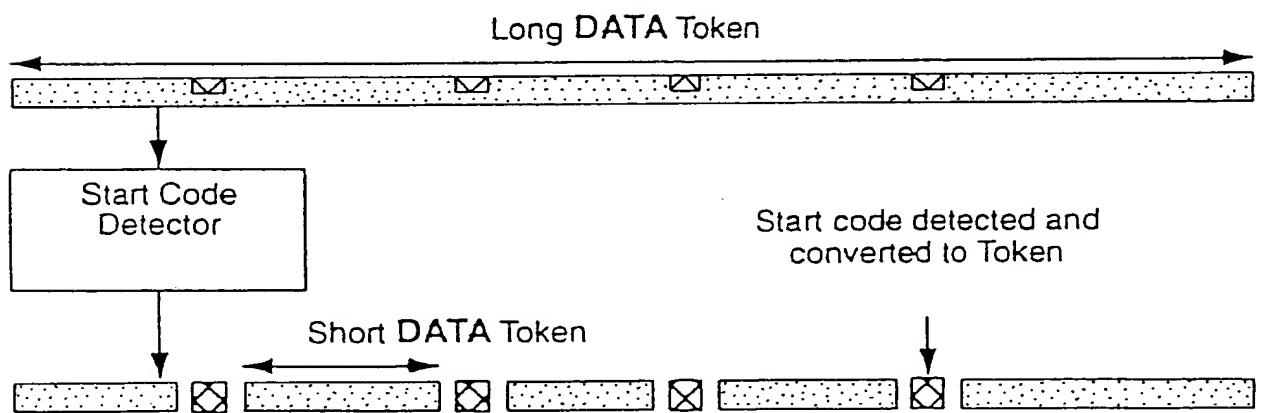


FIG.62

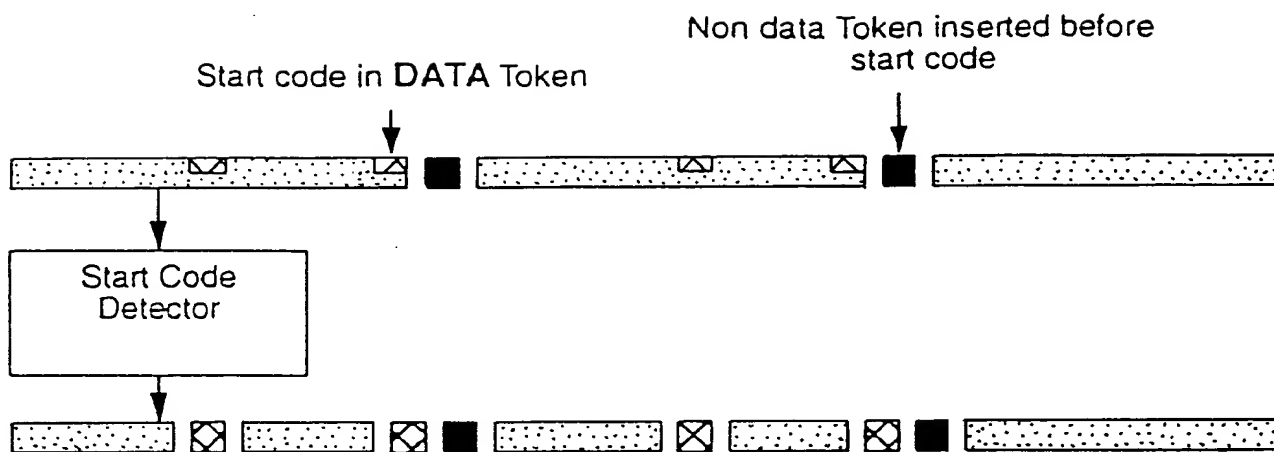


FIG.63

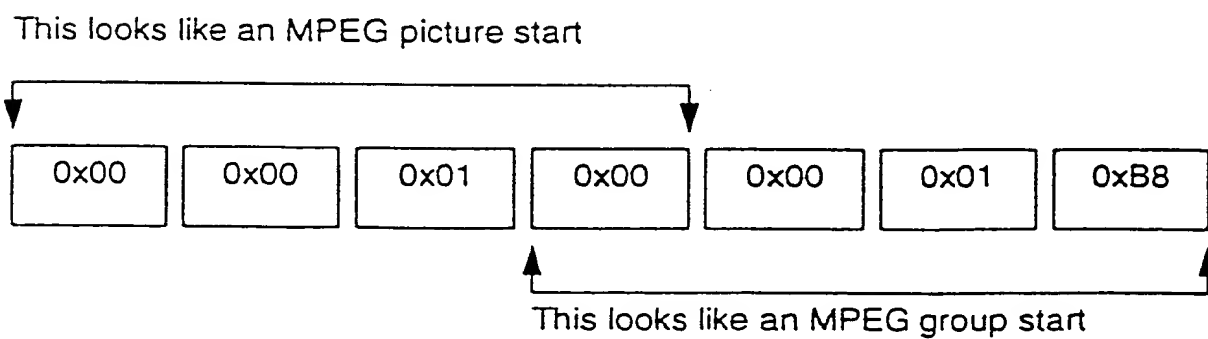


FIG.64

This looks like an MPEG slice start (0x28)

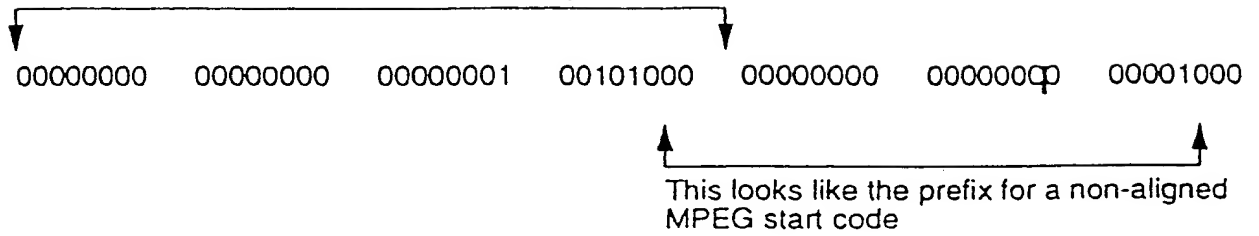


FIG.65

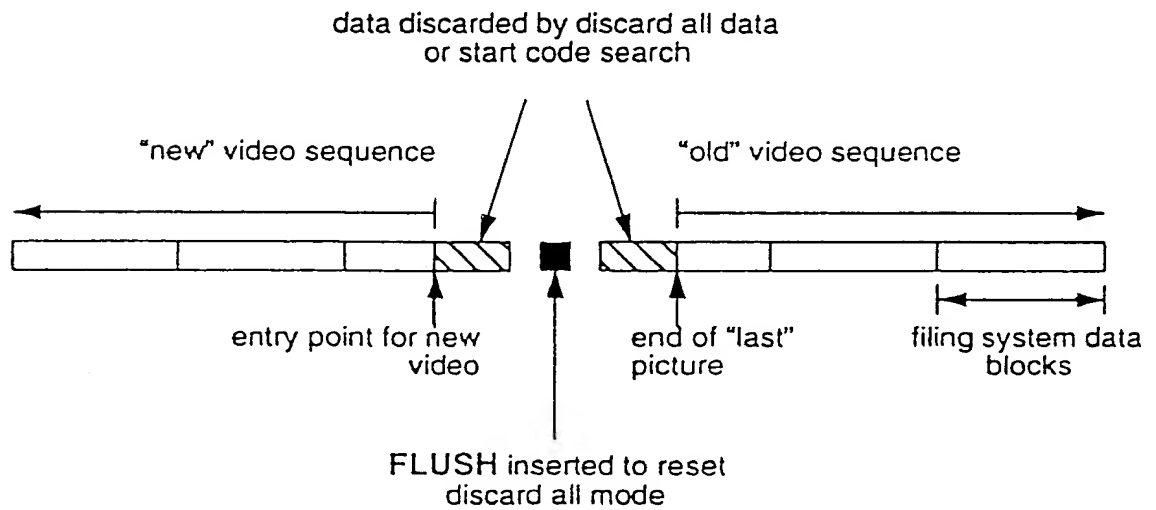


FIG.66

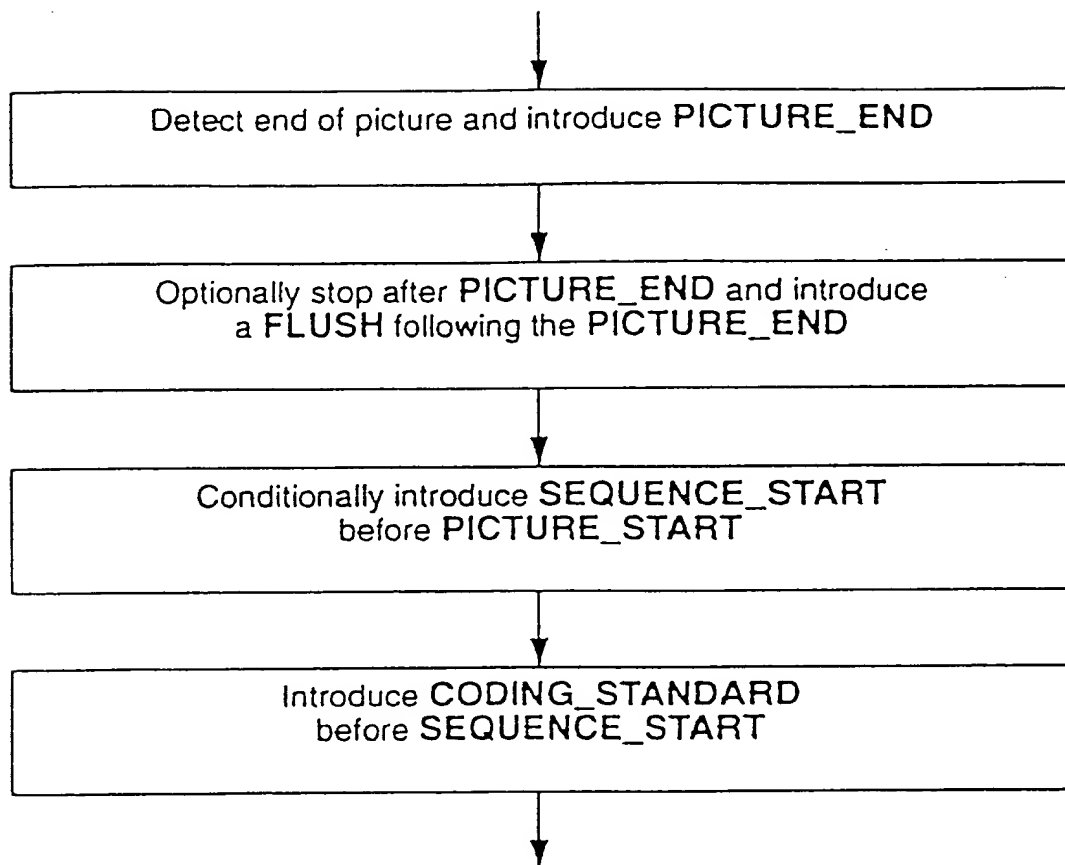


FIG.67

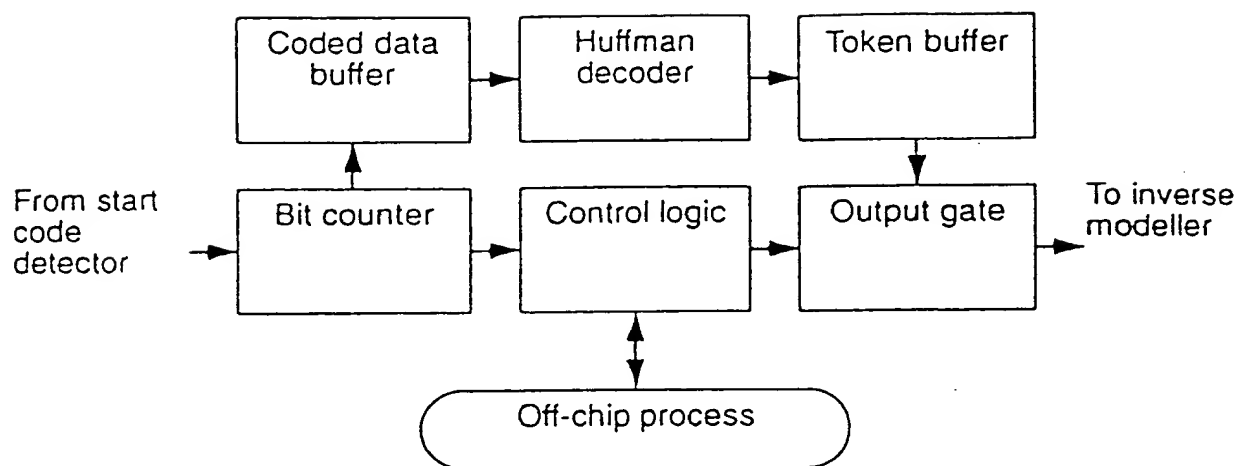


FIG.68

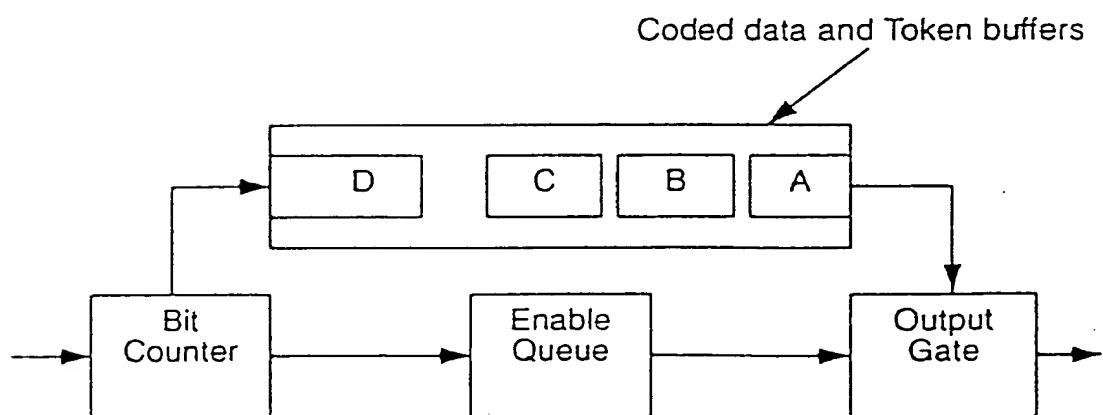


FIG.69

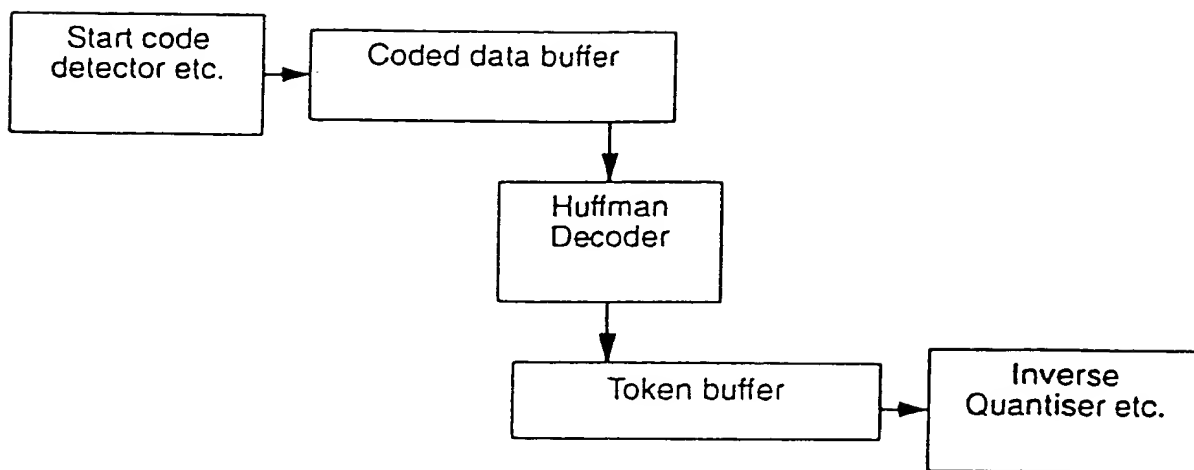


FIG.70

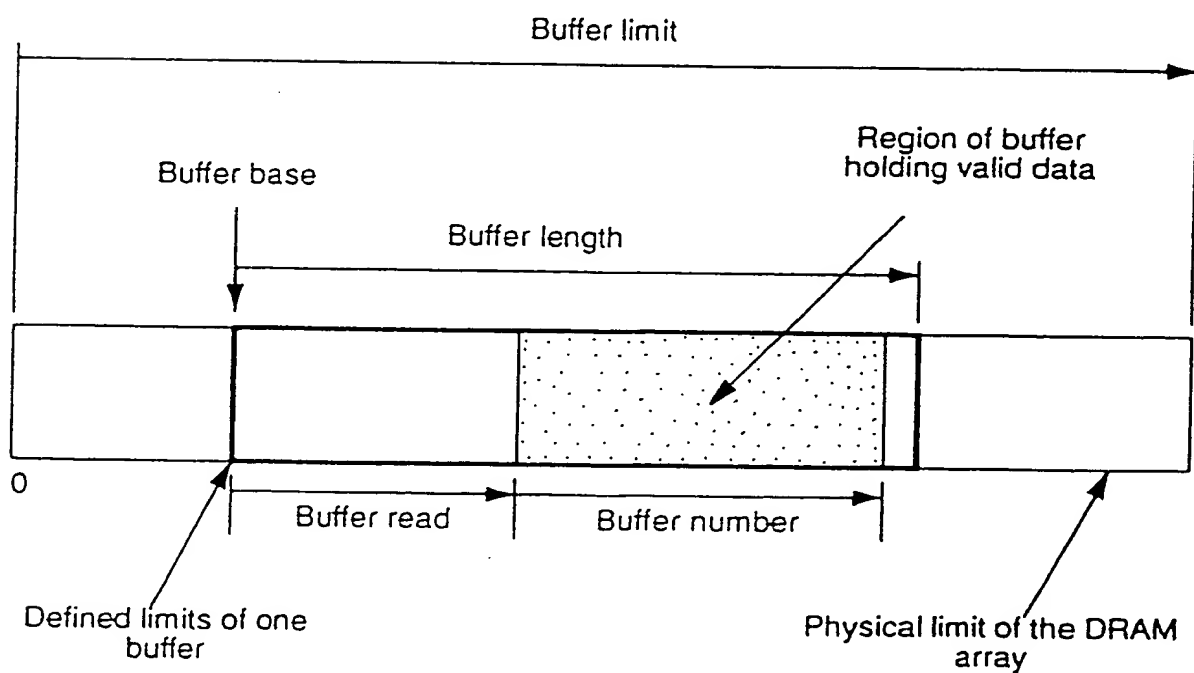


FIG.71

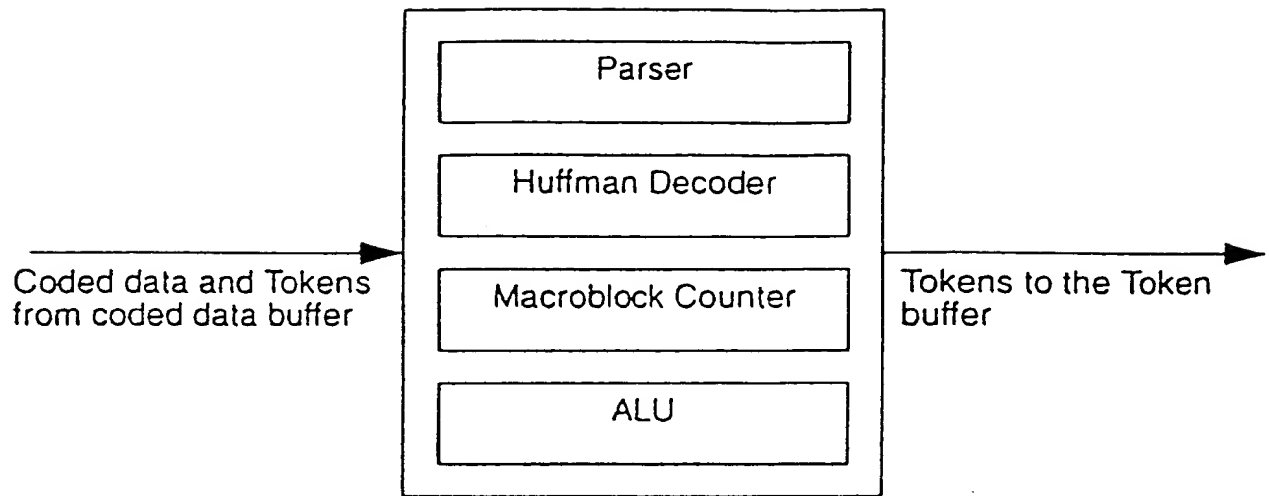


FIG.72

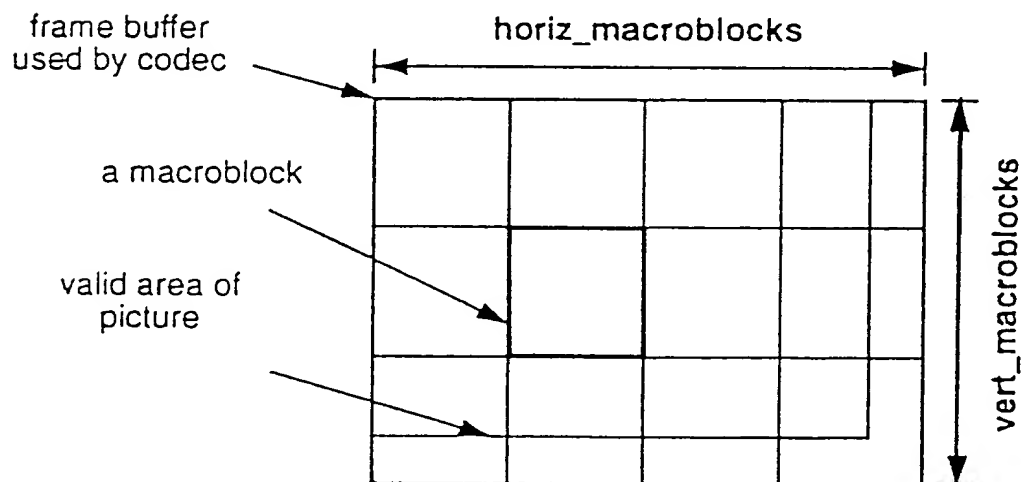


FIG.73

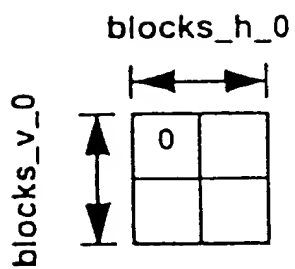


FIG.74A

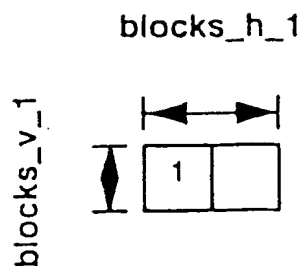


FIG.74B

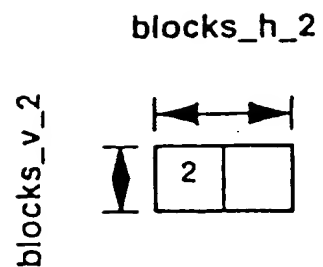


FIG.74C

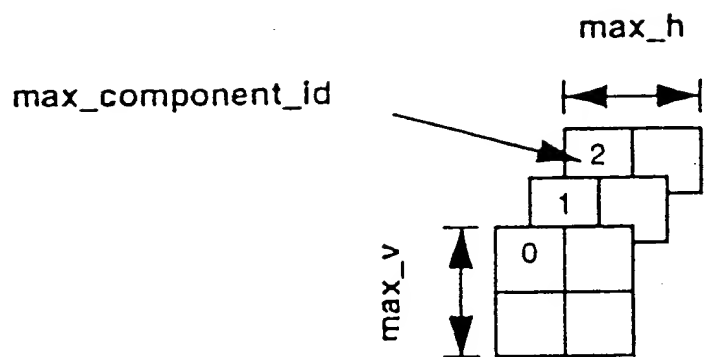


FIG.74D

$$\left\{ \begin{array}{l} \text{horiz_macroblocks} = \frac{\text{horiz_pels} + 15}{16} \\ \text{vert_macroblocks} = \frac{\text{vert_pels} + 15}{16} \end{array} \right.$$

FIG.75

From Token buffer

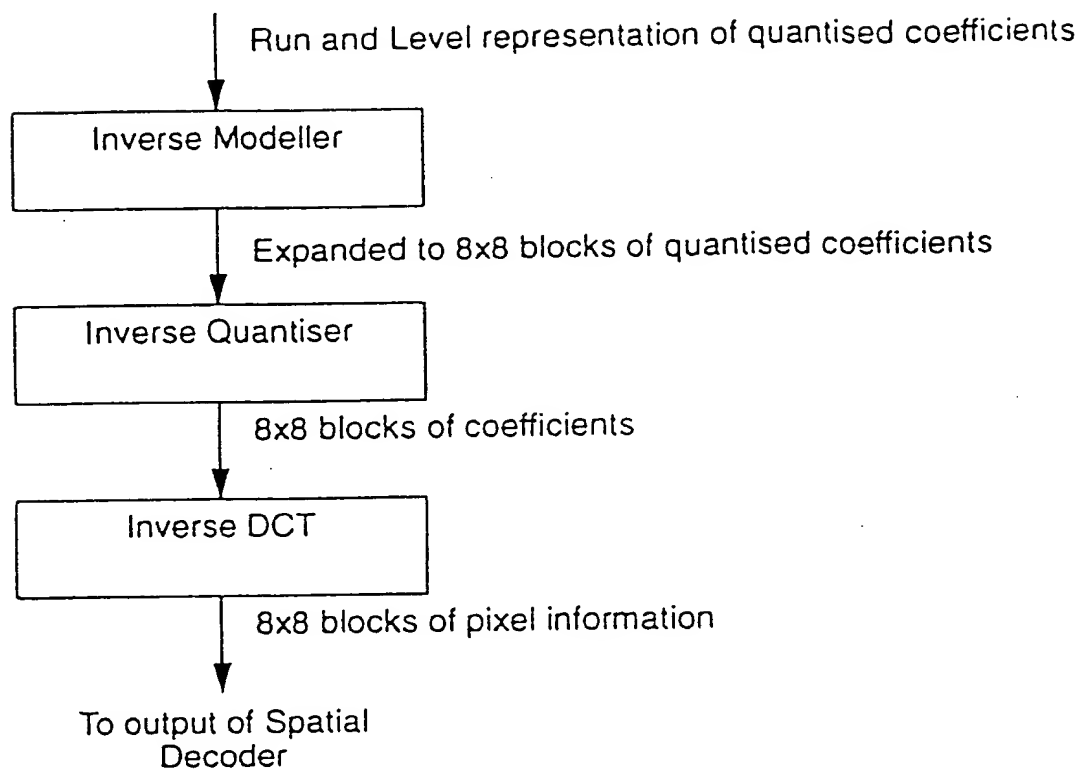


FIG.76

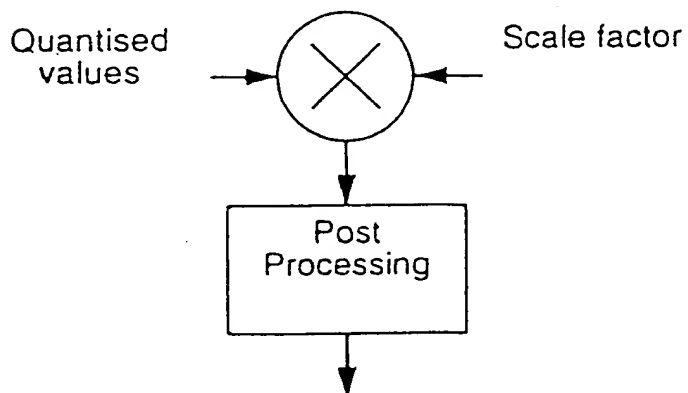


FIG.77

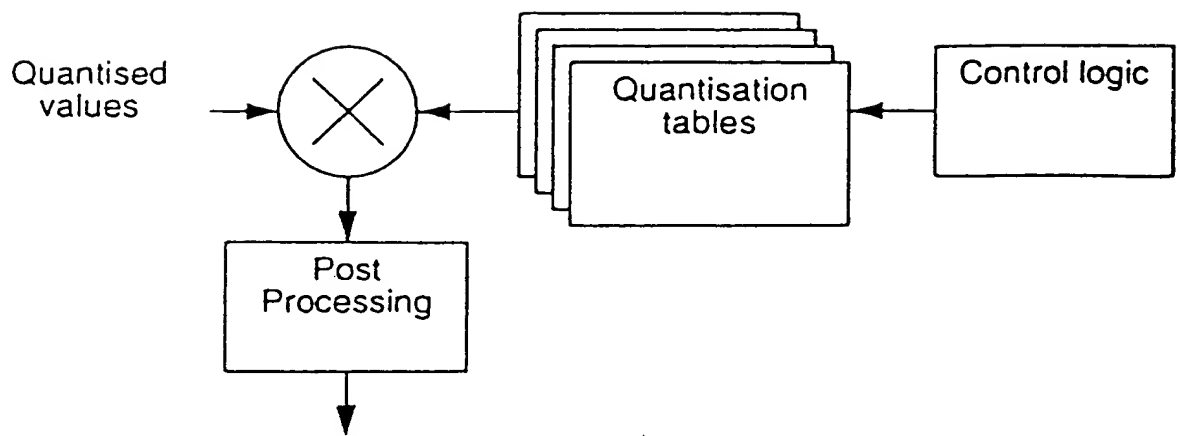


FIG.78

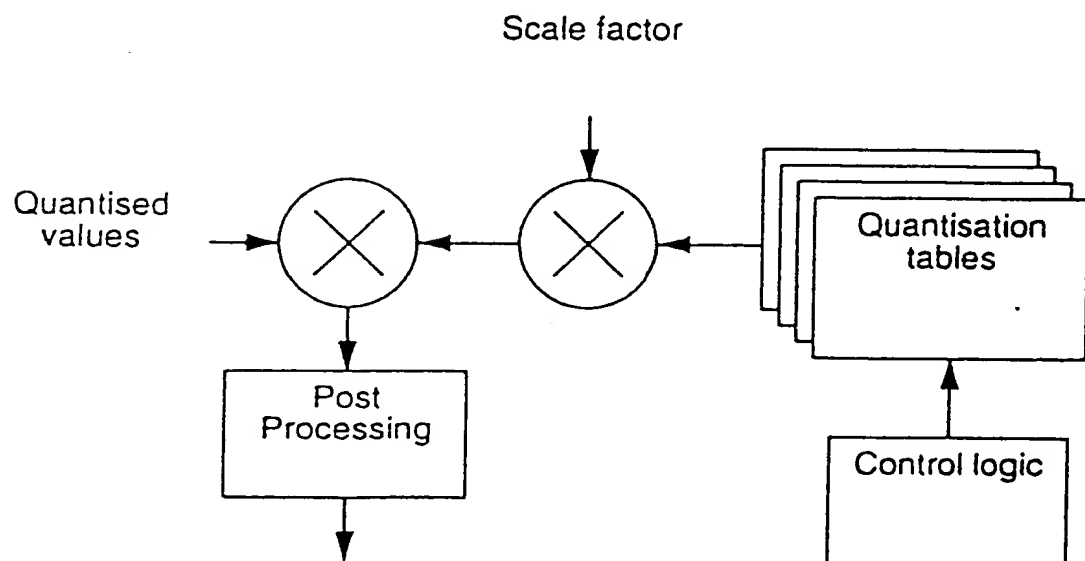


FIG.79

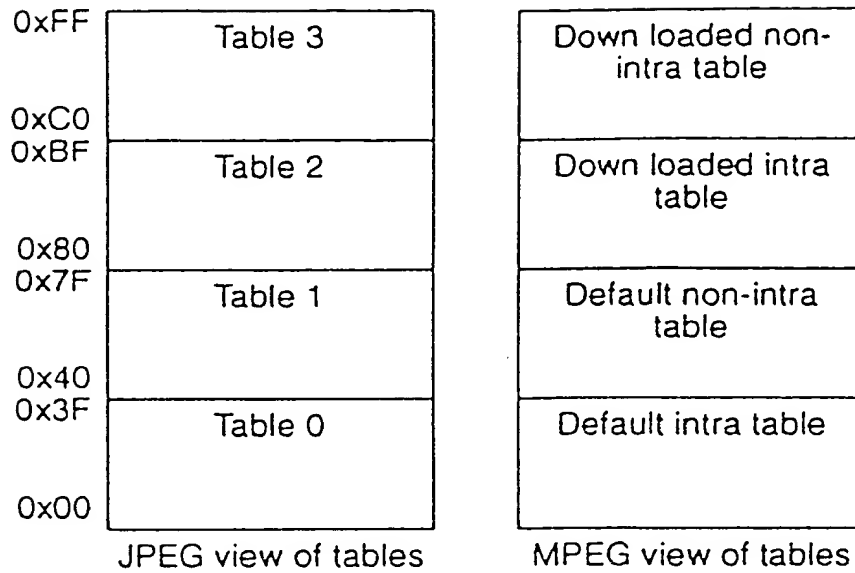


FIG.80

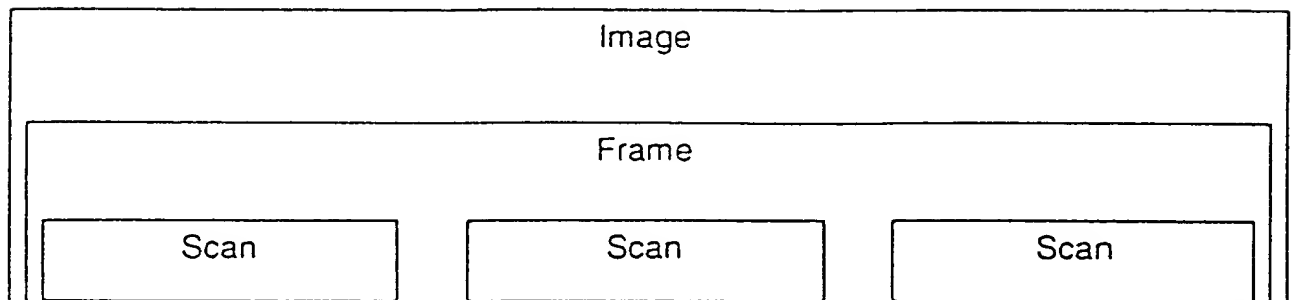


FIG.81

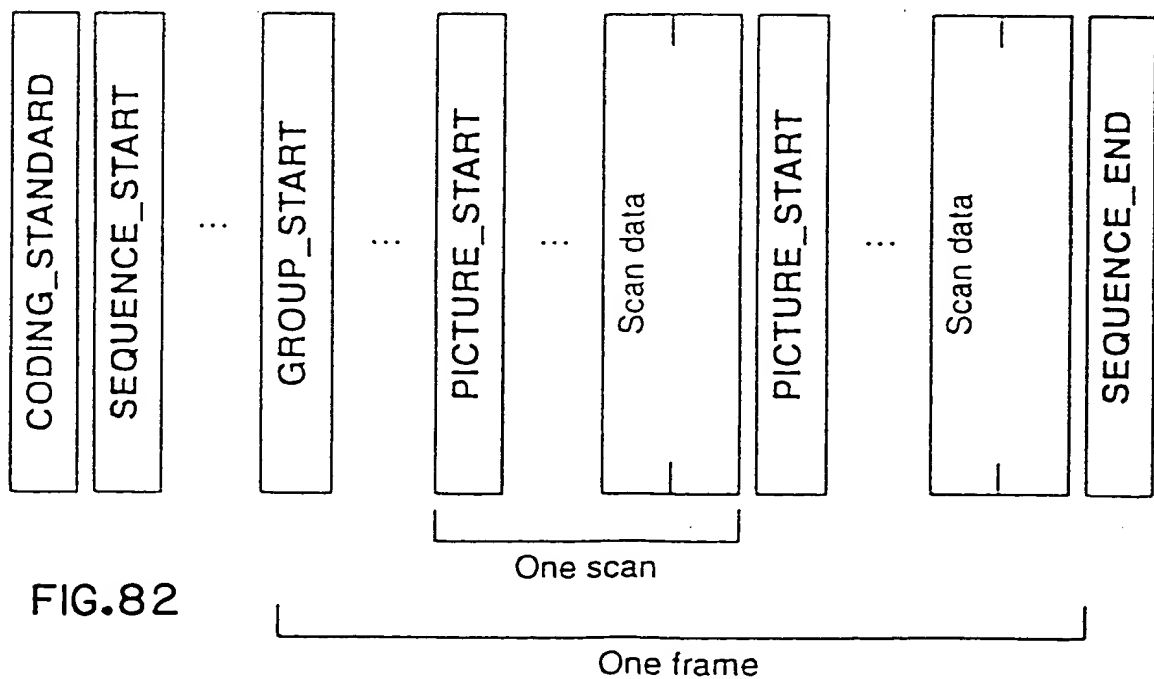


FIG.82

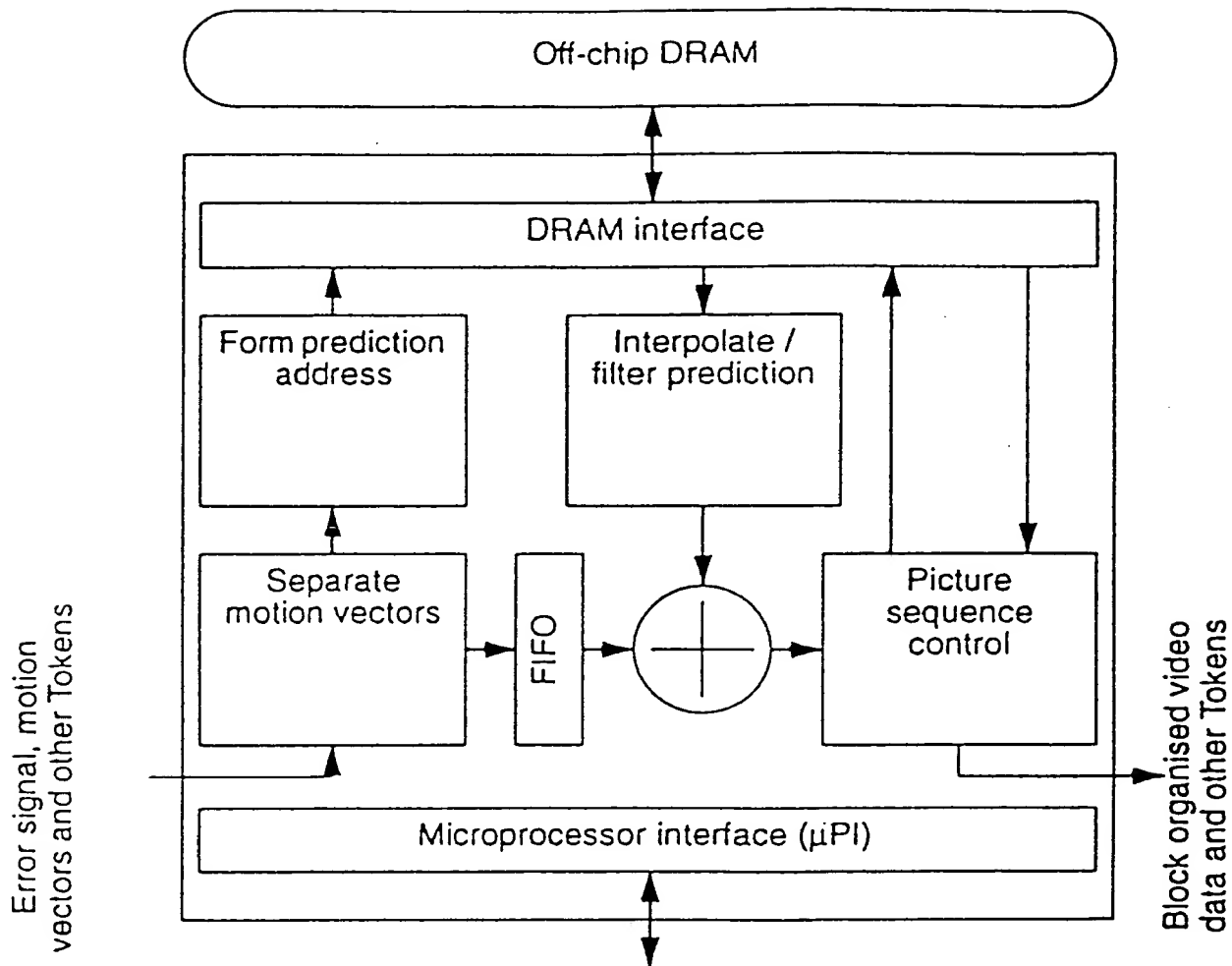


FIG.83

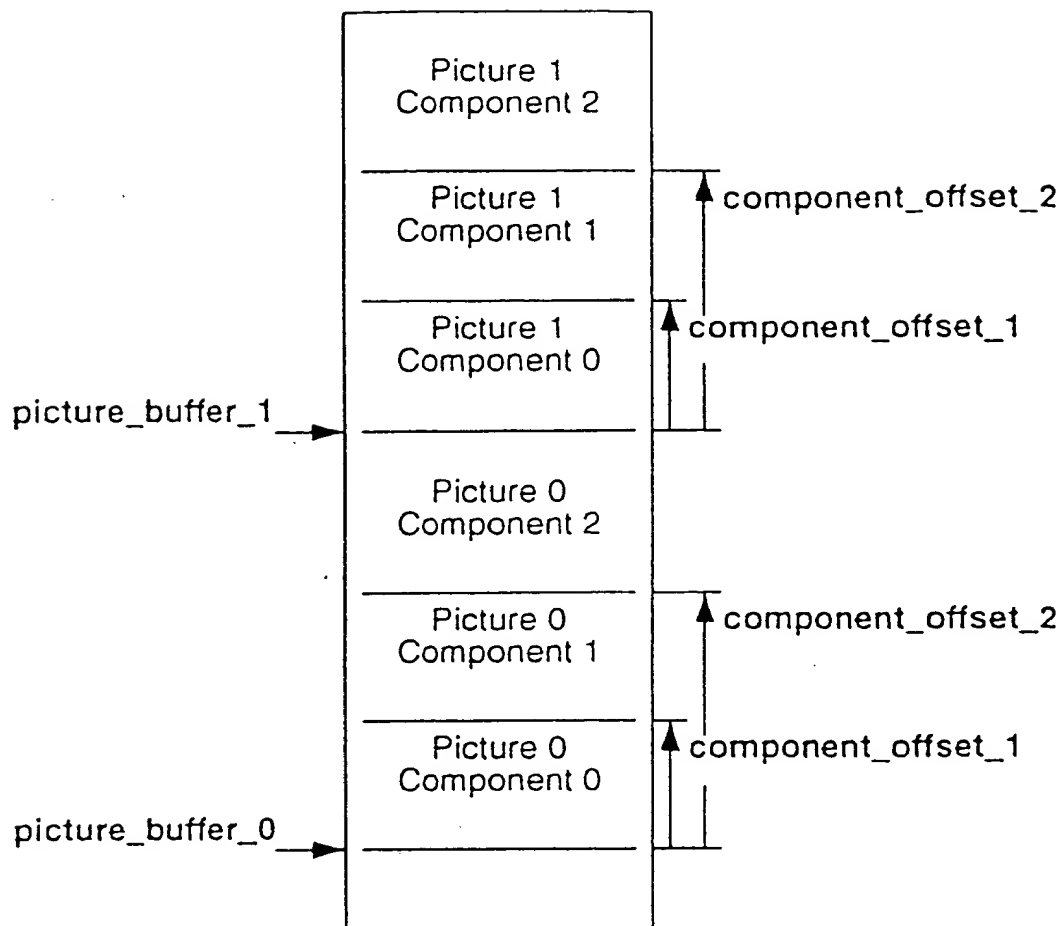


FIG.84

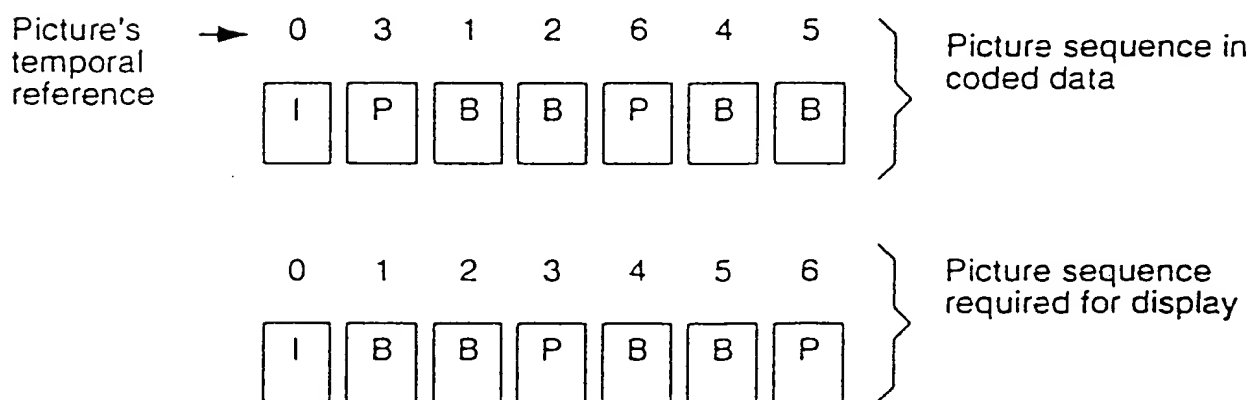


FIG.85

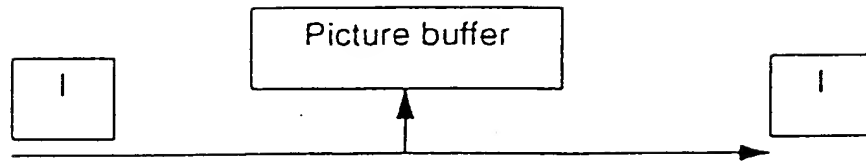


FIG.86

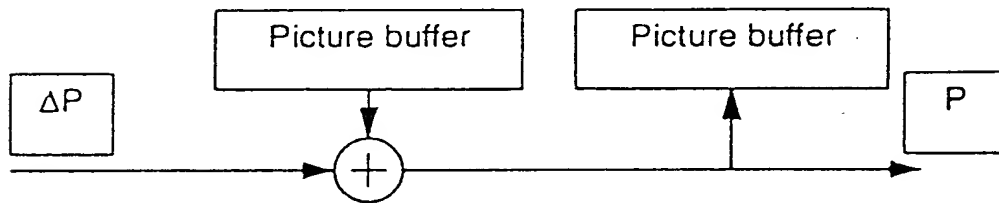


FIG.87

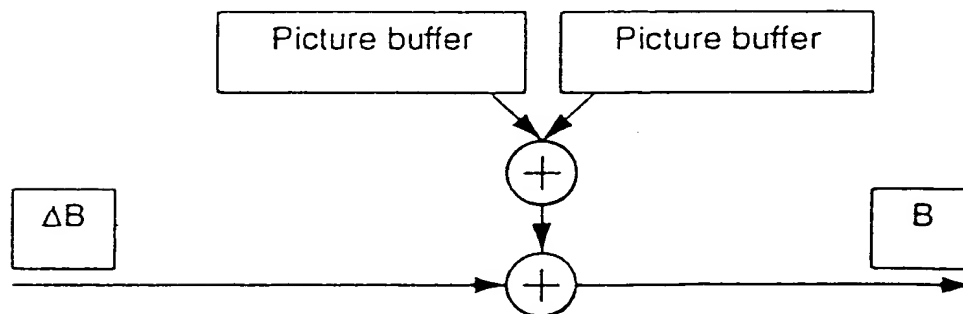


FIG.88

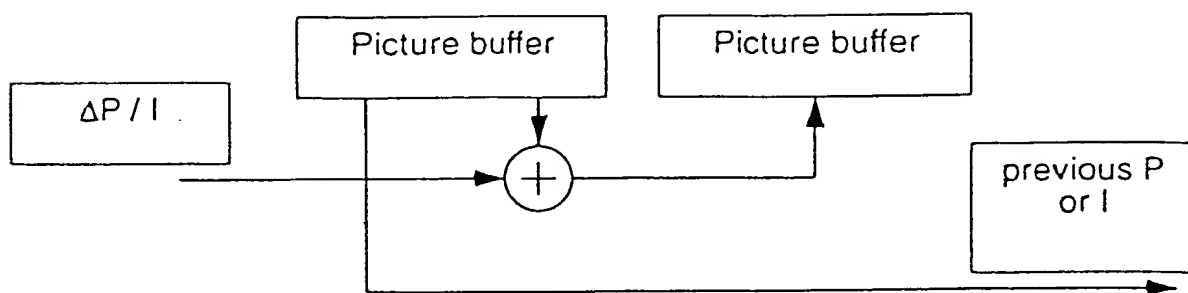


FIG.89

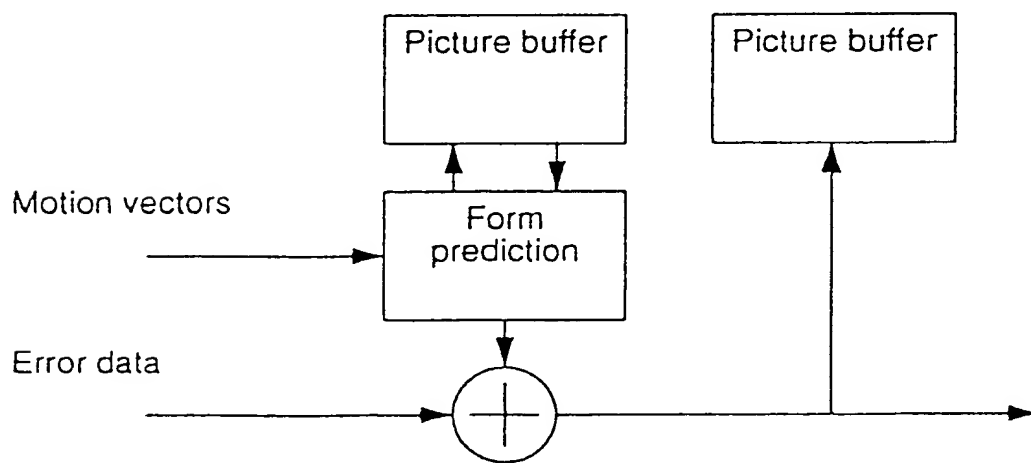


FIG.90

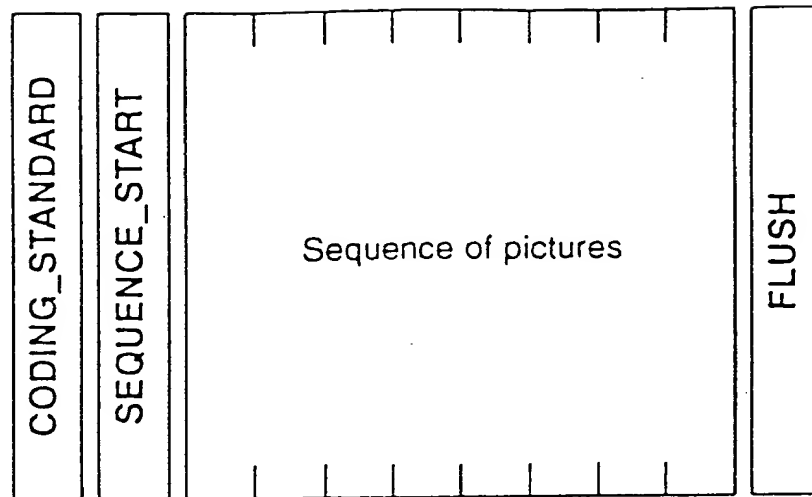


FIG.91

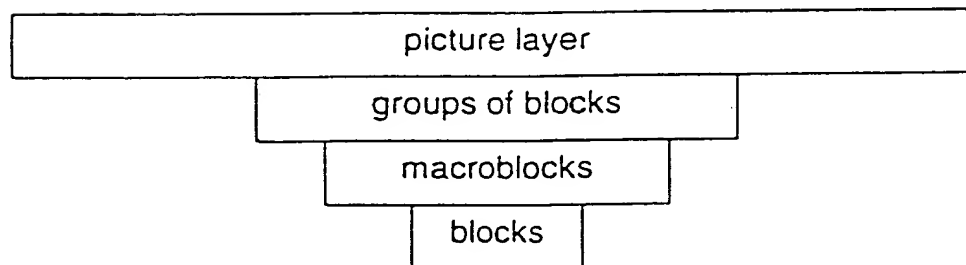


FIG.92

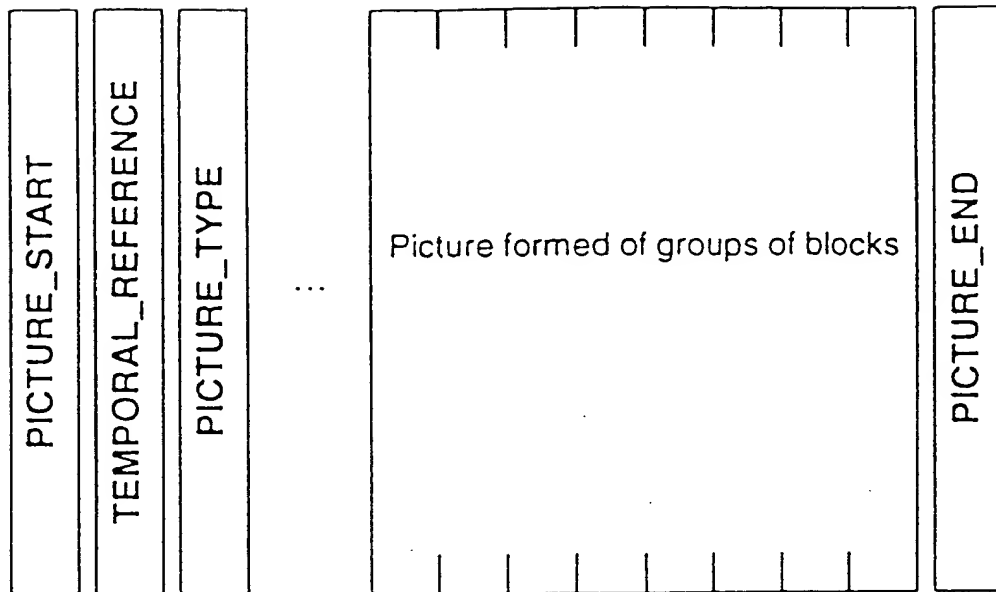


FIG.93

CIF		QCIF
0	1	0
2	3	2
4	5	4
6	7	
8	9	
10	11	

FIG.94

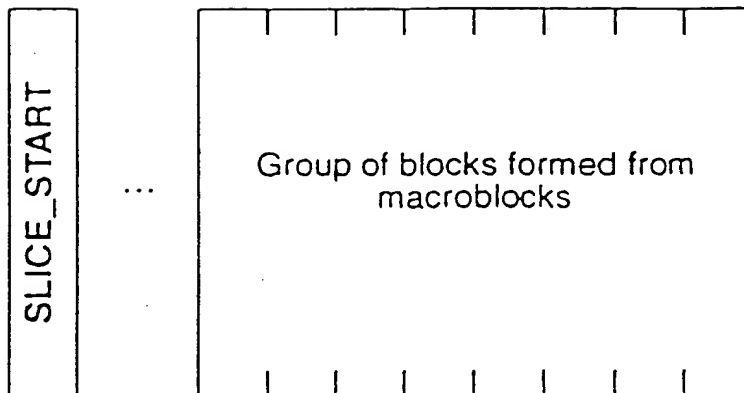


FIG.95

1	2	3	4	5	6	7	8	9	10	11
12	13	14	15	16	17	18	19	20	21	22
23	24	25	26	27	28	29	30	31	32	33

FIG.96

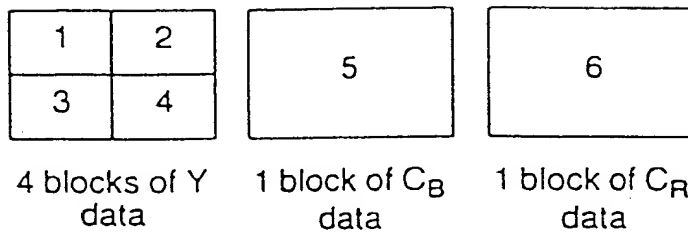


FIG.97

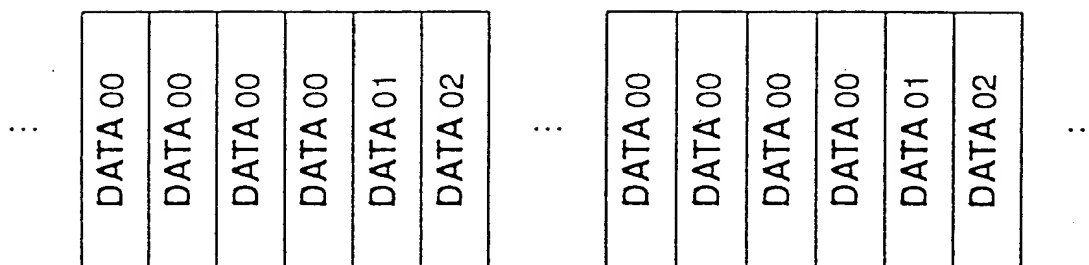


FIG.98

1	2	3	4	5	6	7	8
9	10	11	12	13	14	15	16

⋮

59	58	59	60	61	62	63	64
----	----	----	----	----	----	----	----

FIG.99

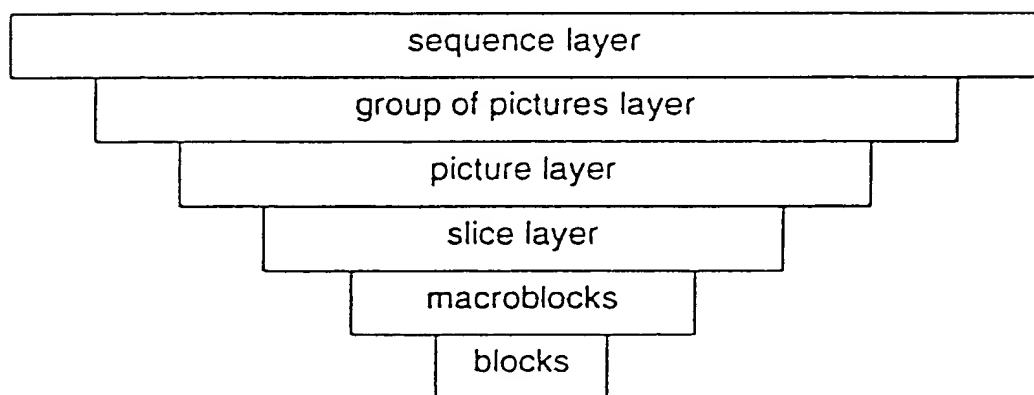


FIG.100

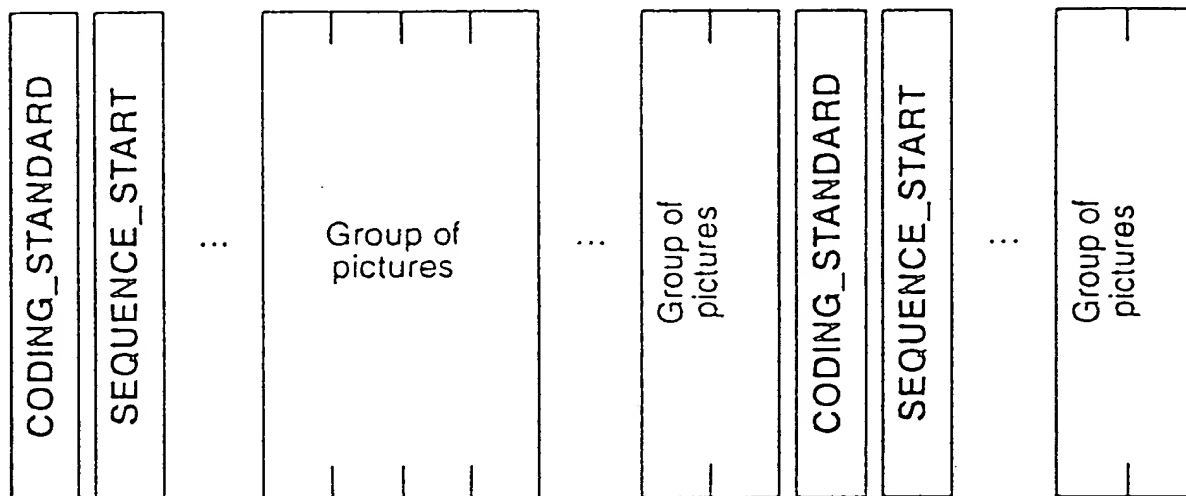


FIG. 101

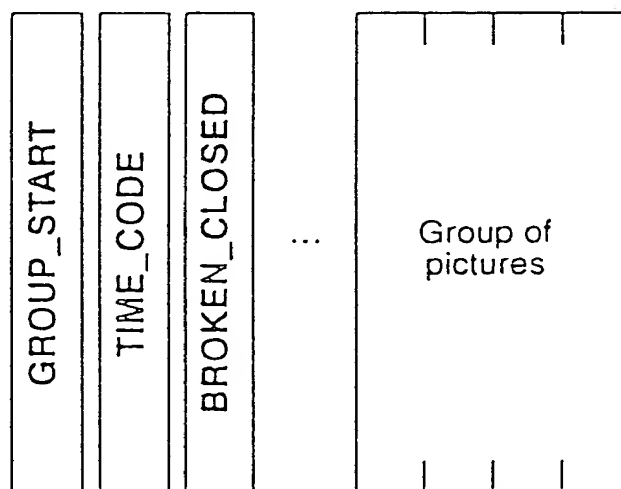


FIG. 102

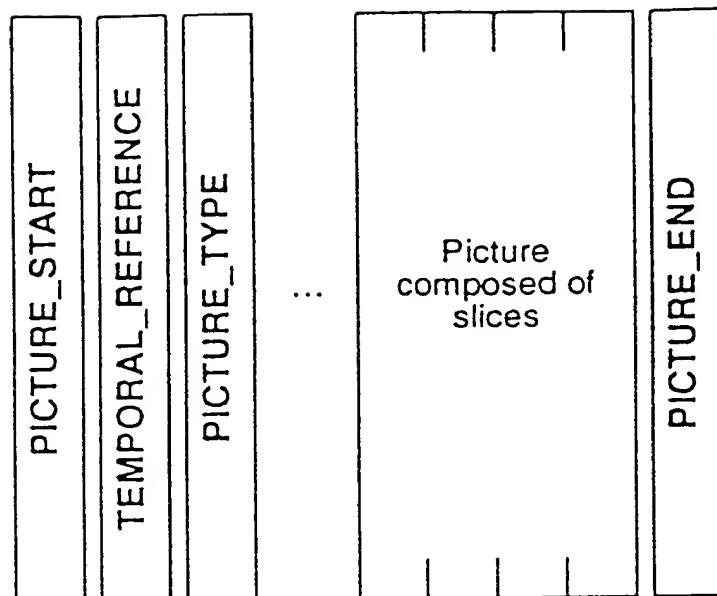


FIG. 103

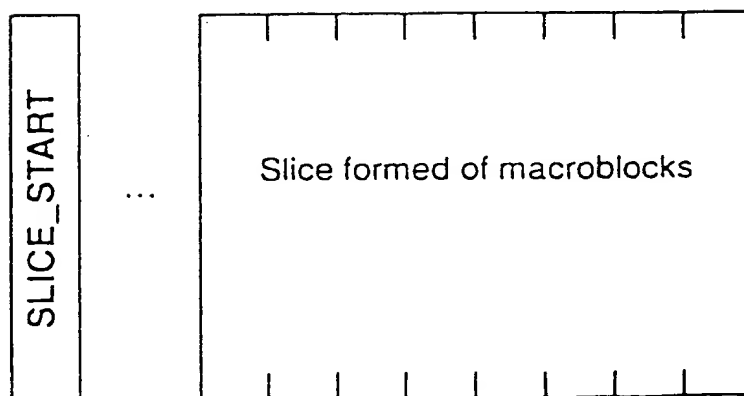


FIG. 104

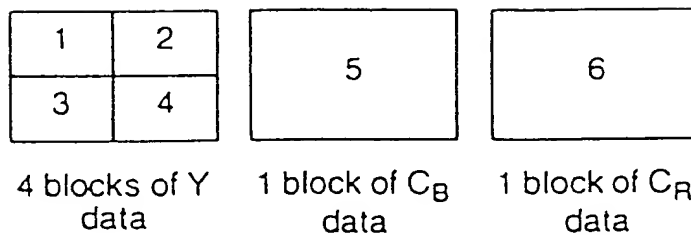


FIG. 105

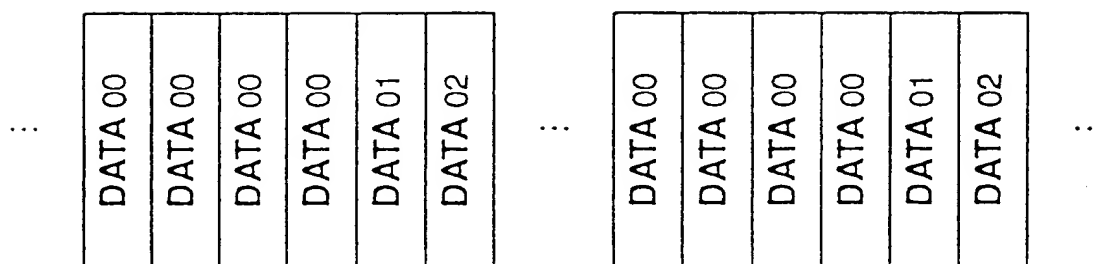


FIG. 106

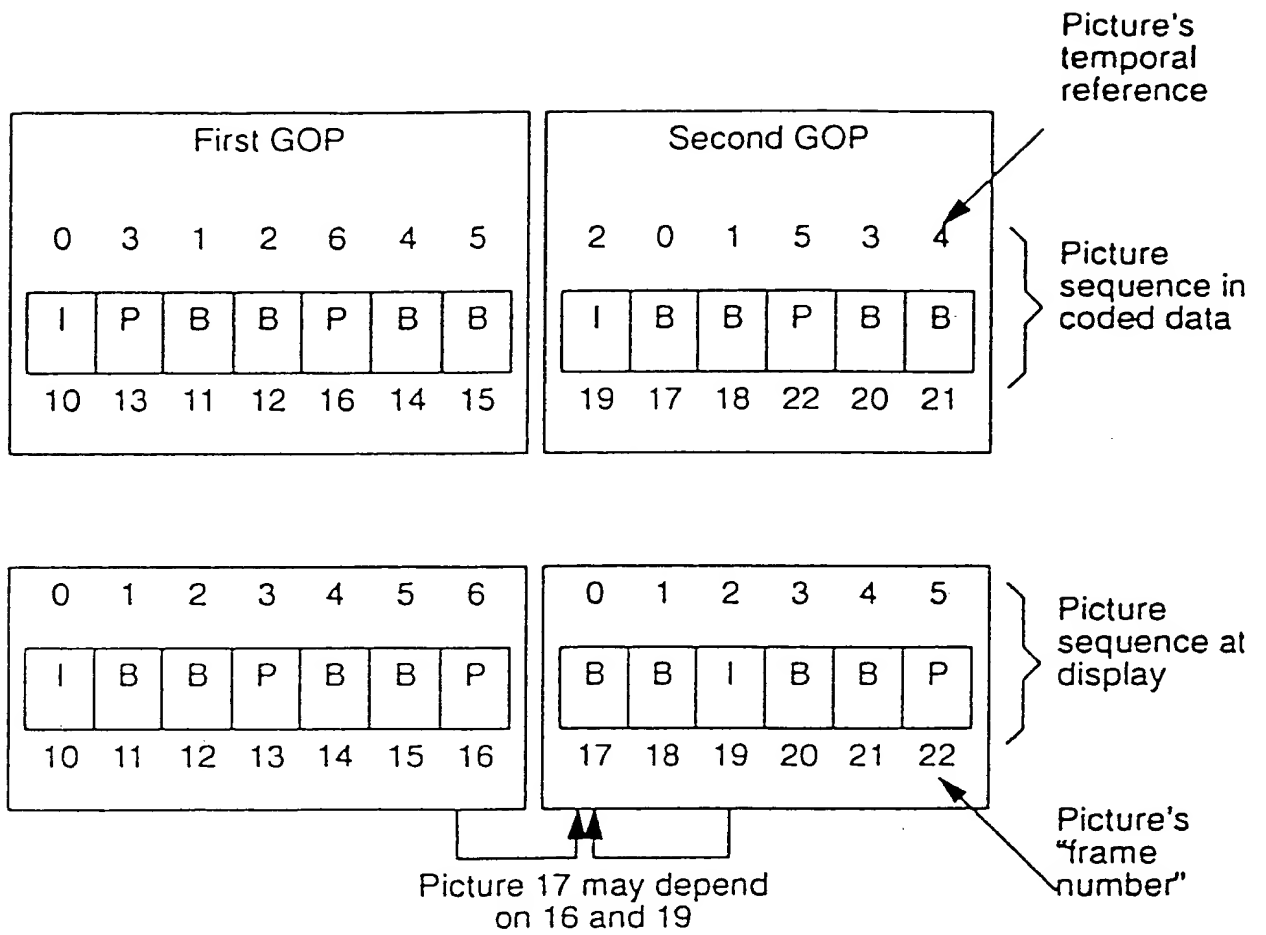


FIG. 107



Access Start

Data Transfer

Default State

FIG. 108

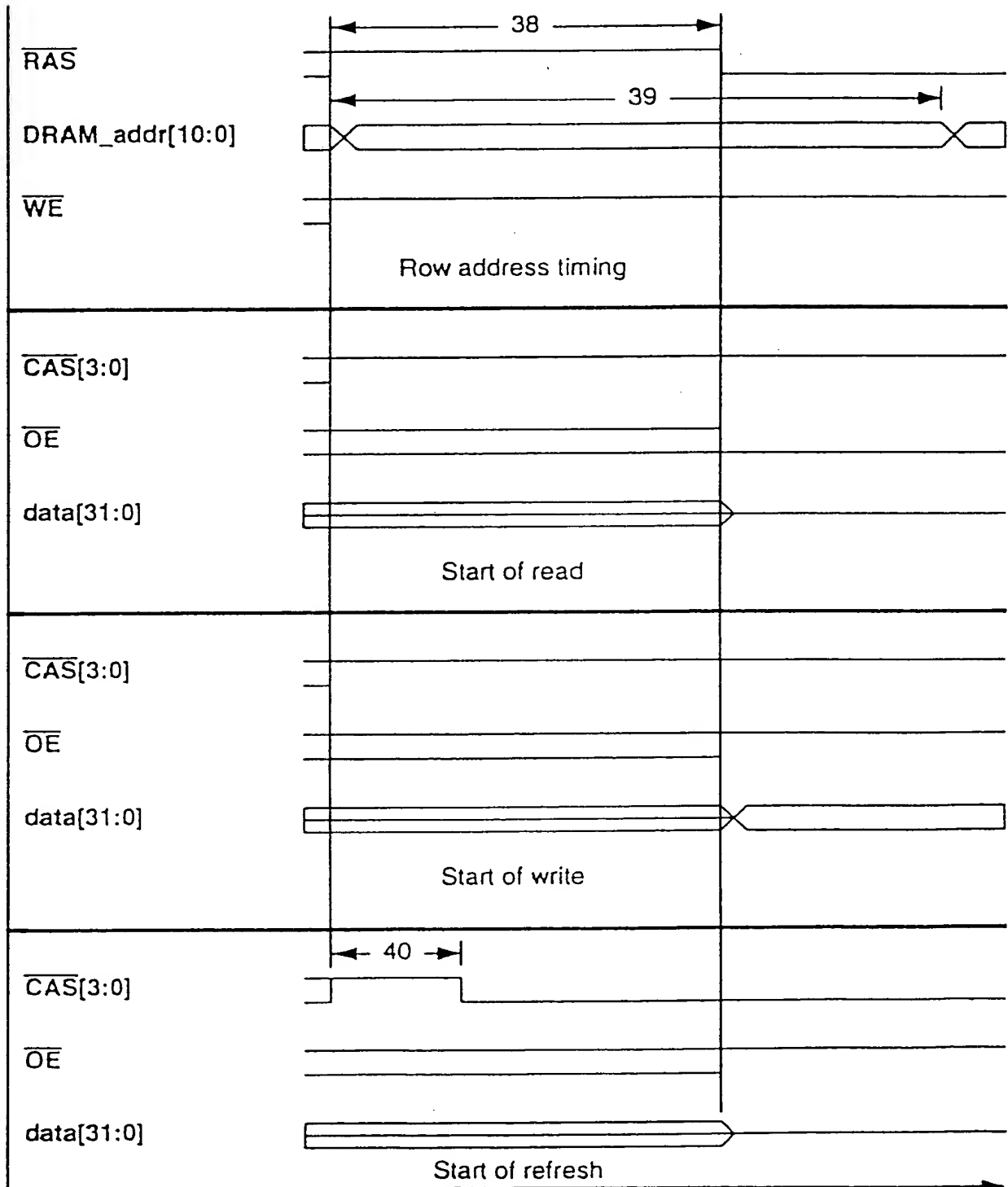


FIG. 109

TIME

$\overline{\text{RAS}}$

DRAM_addr[10:0]

$\overline{\text{CAS}}[3:0]$

$\overline{\text{WE}}$

$\overline{\text{OE}}$

DRAM_data[31:0]

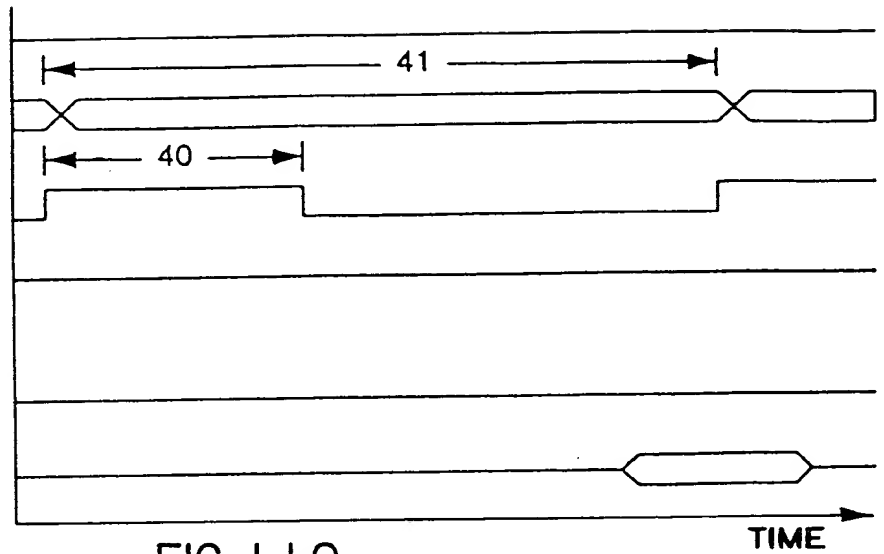


FIG. 110

$\overline{\text{RAS}}$

DRAM_addr[10:0]

$\overline{\text{CAS}}[3:0]$

$\overline{\text{WE}}$

$\overline{\text{OE}}$

DRAM_data[31:0]

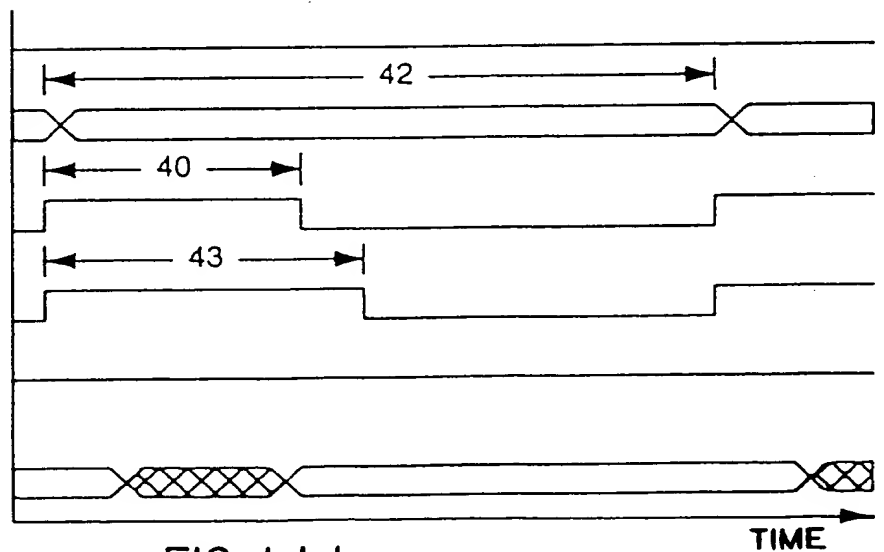


FIG. 111

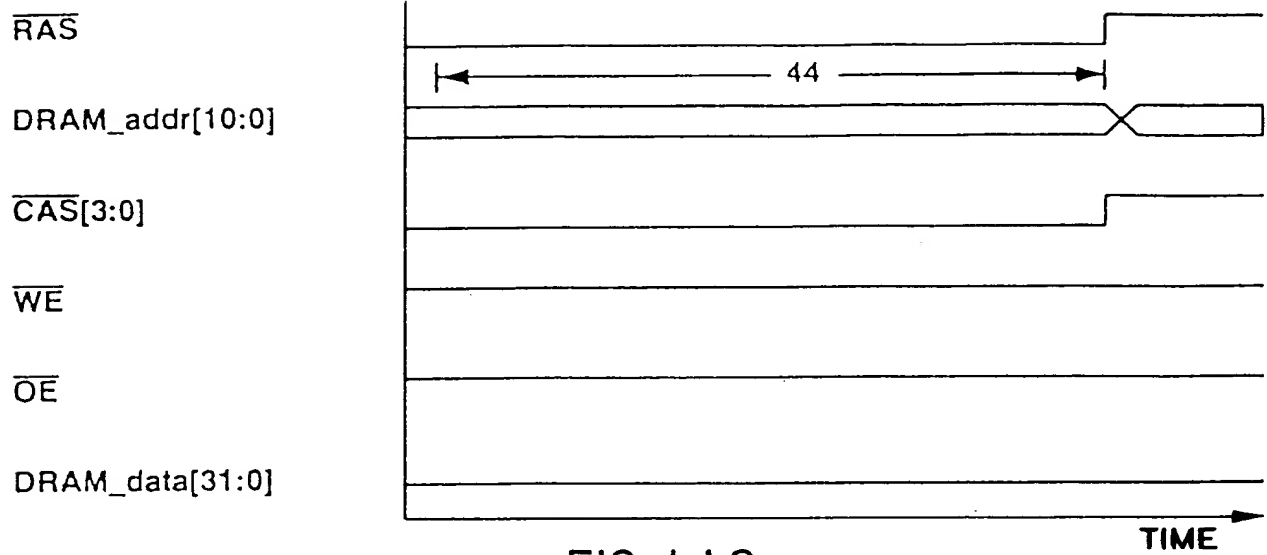


FIG. 112

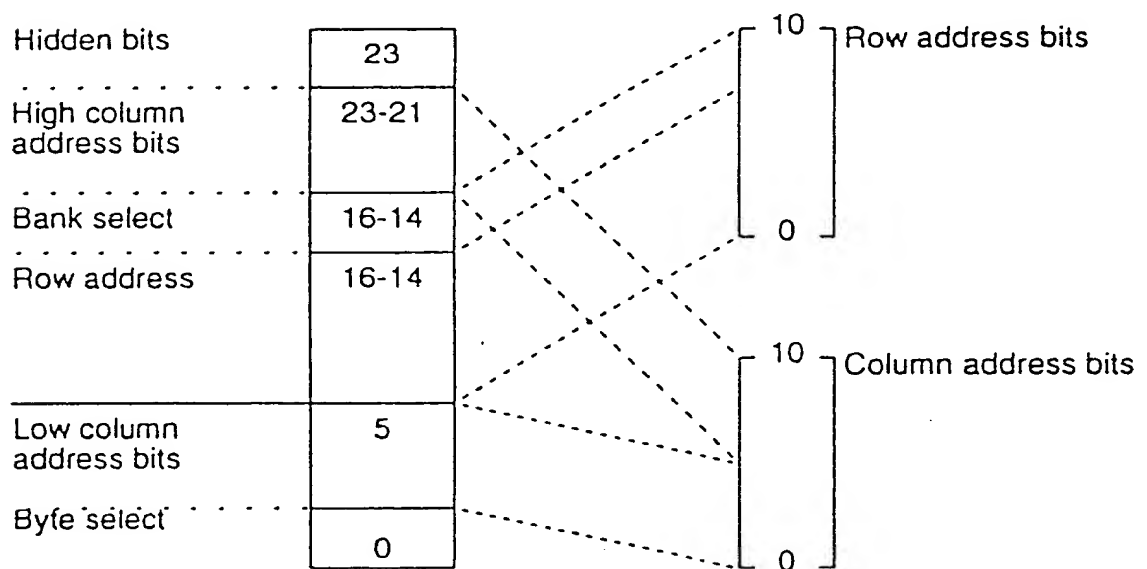


FIG. 113

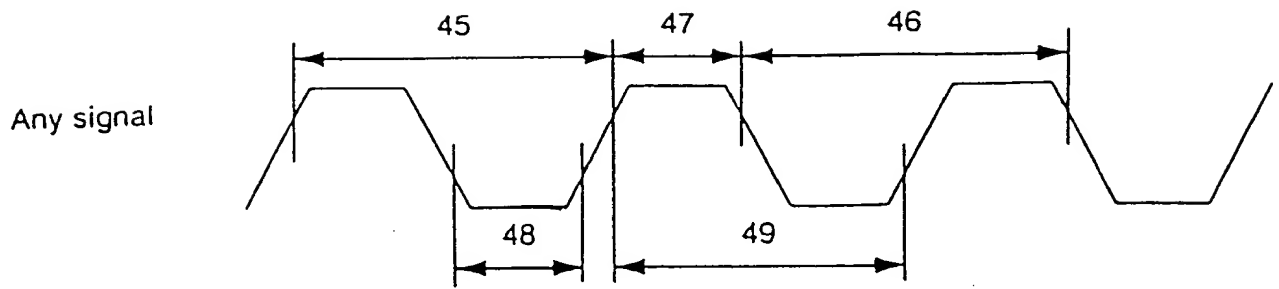


FIG. 114

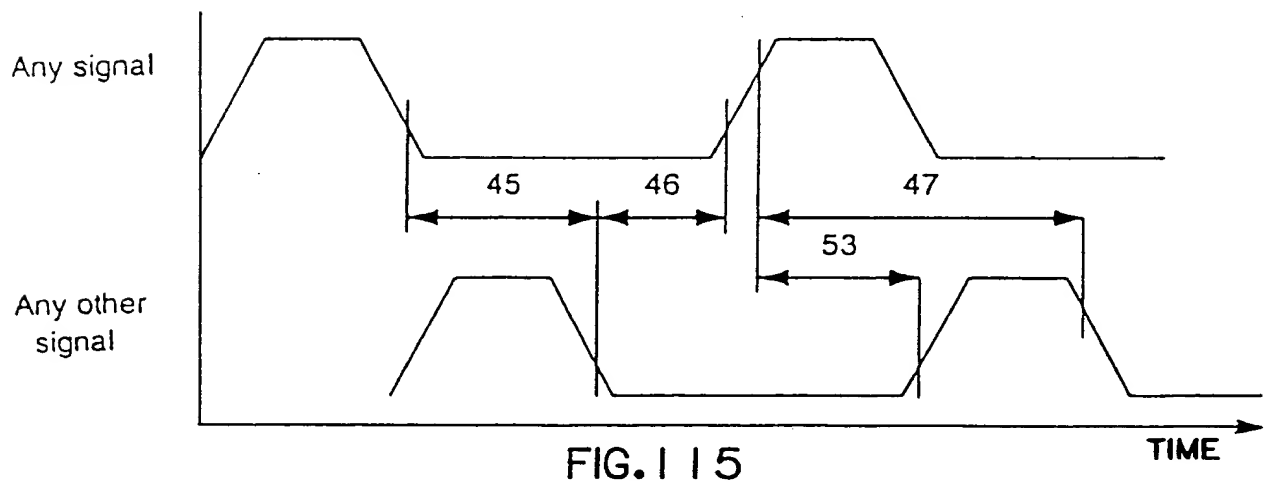


FIG. 115

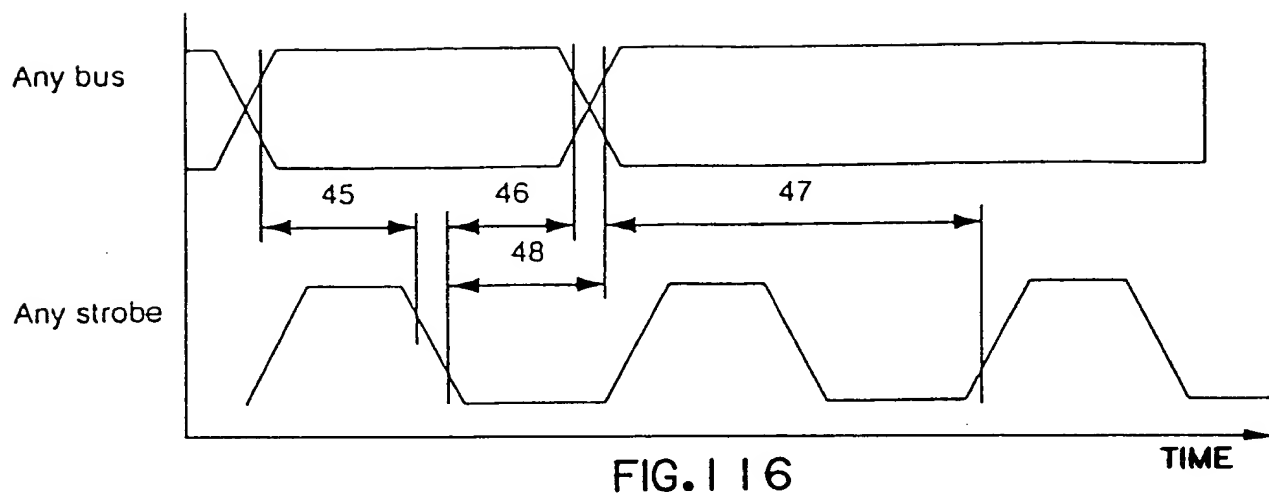


FIG. 116

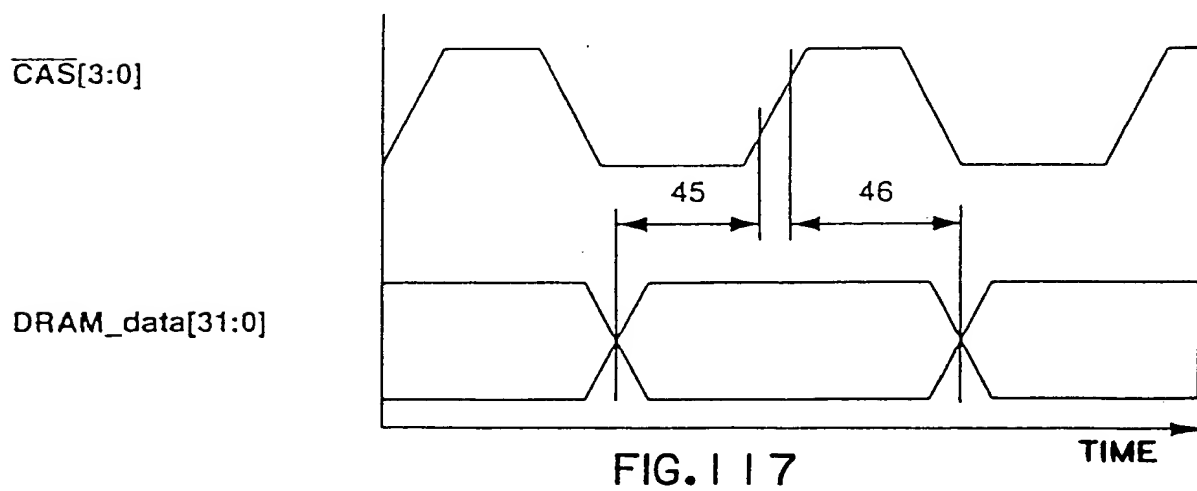


FIG. 117

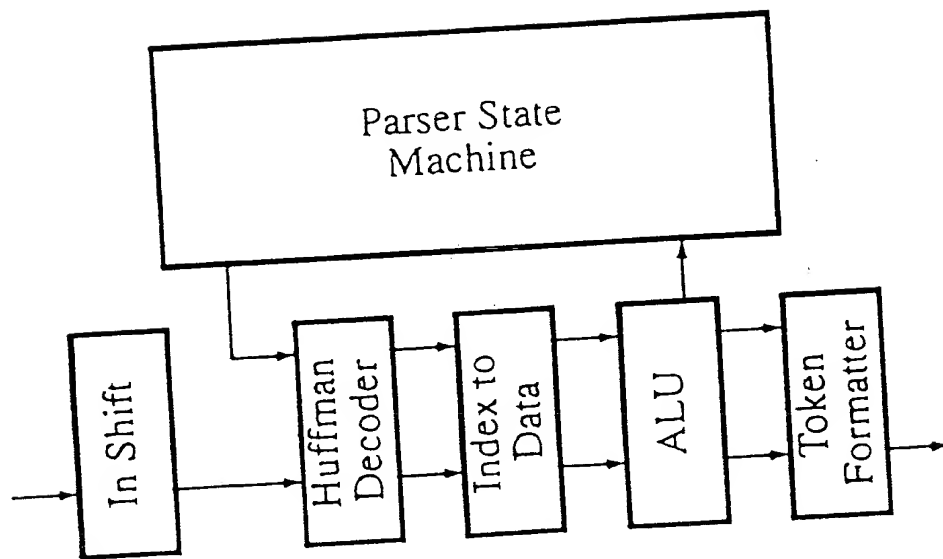


FIG. 118

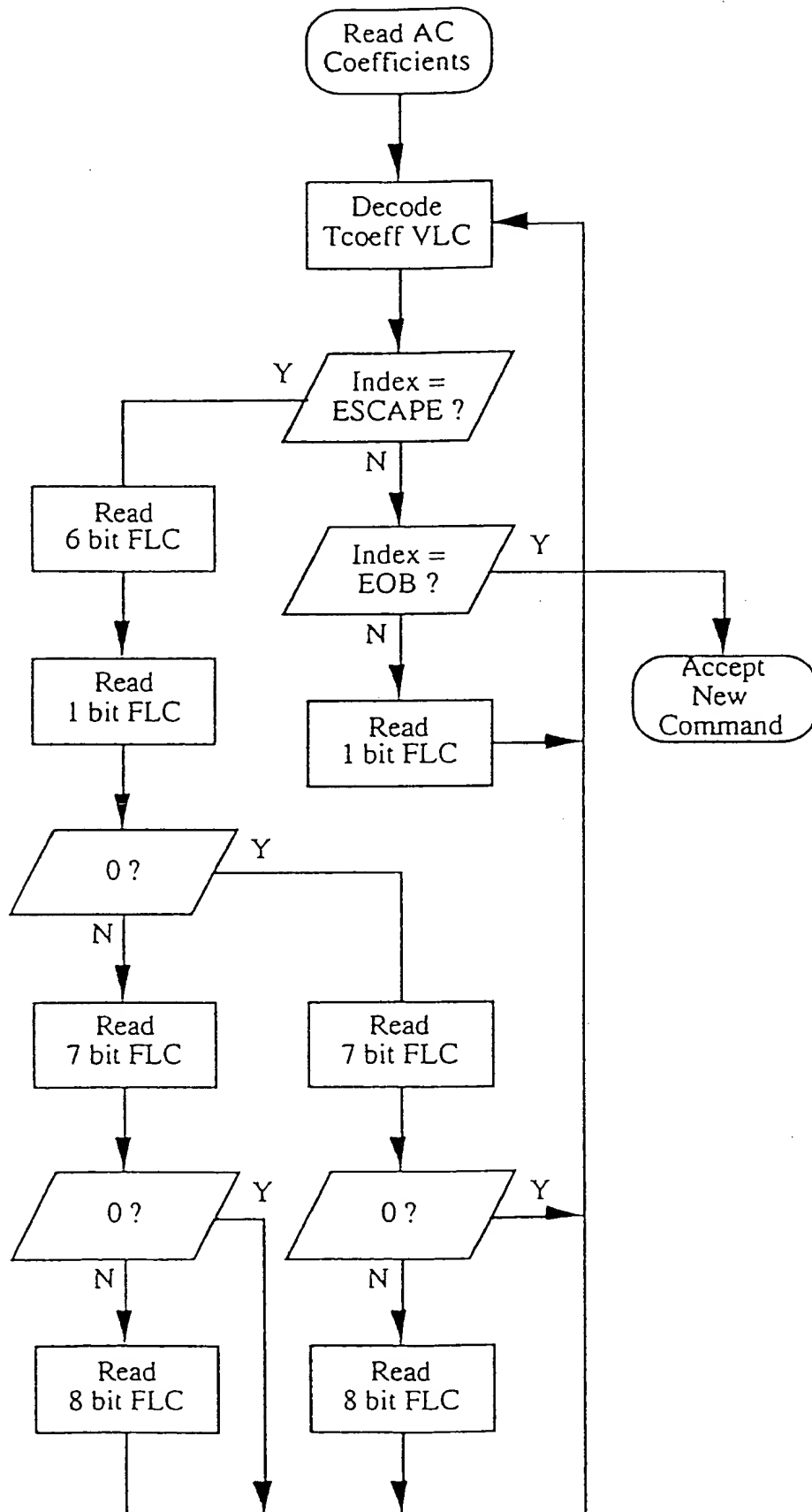


FIG. 119

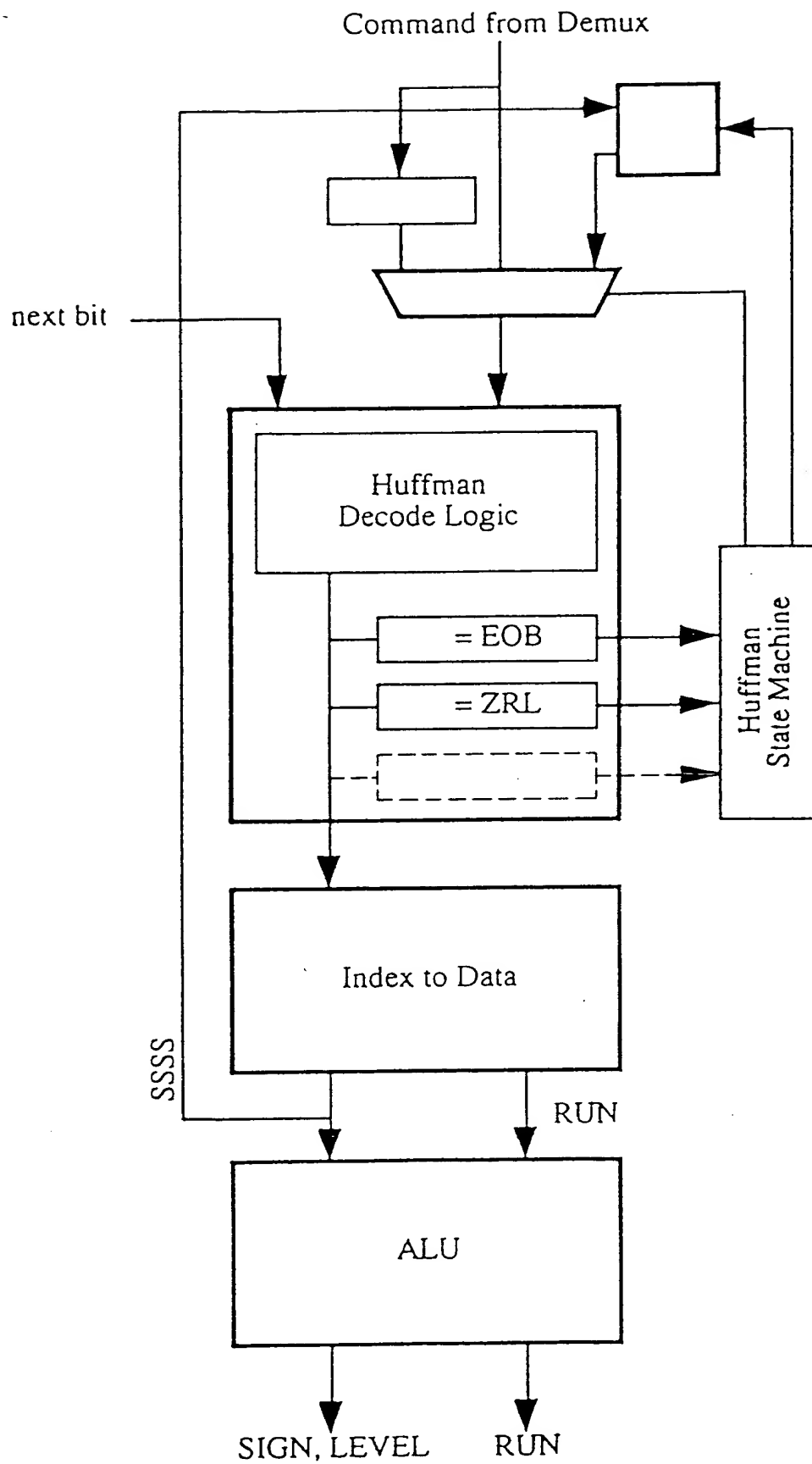


FIG. 120

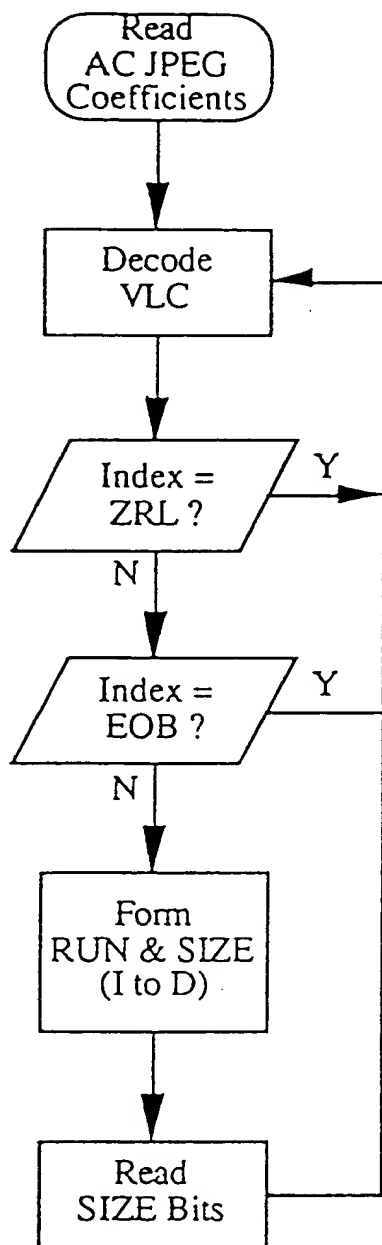


FIG. 121A

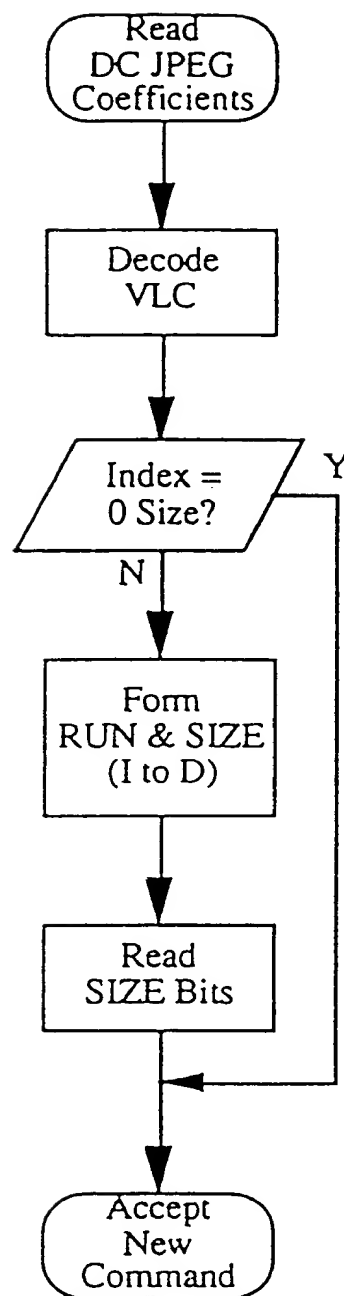


FIG. 121B

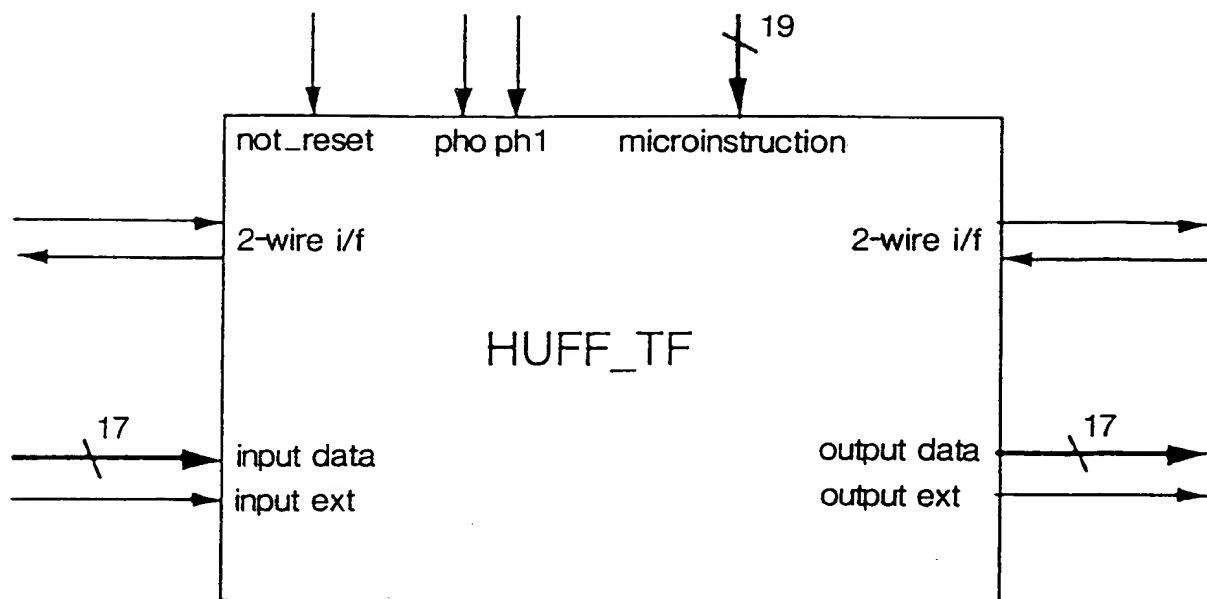


FIG. 122

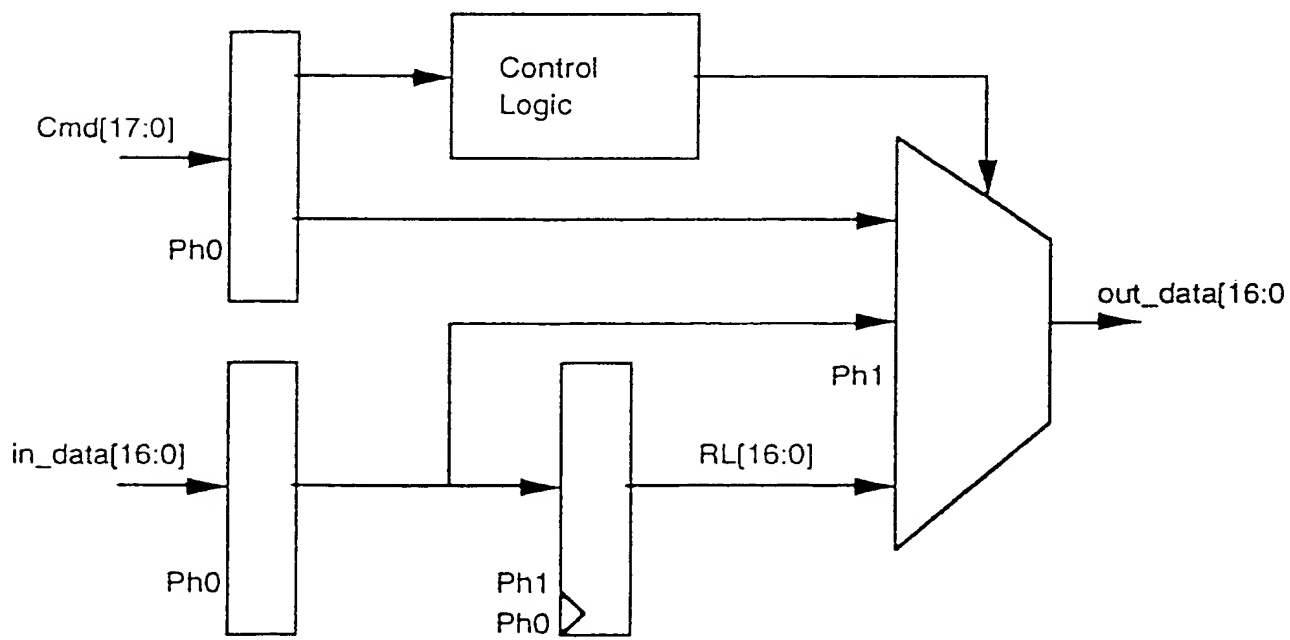


FIG. 123

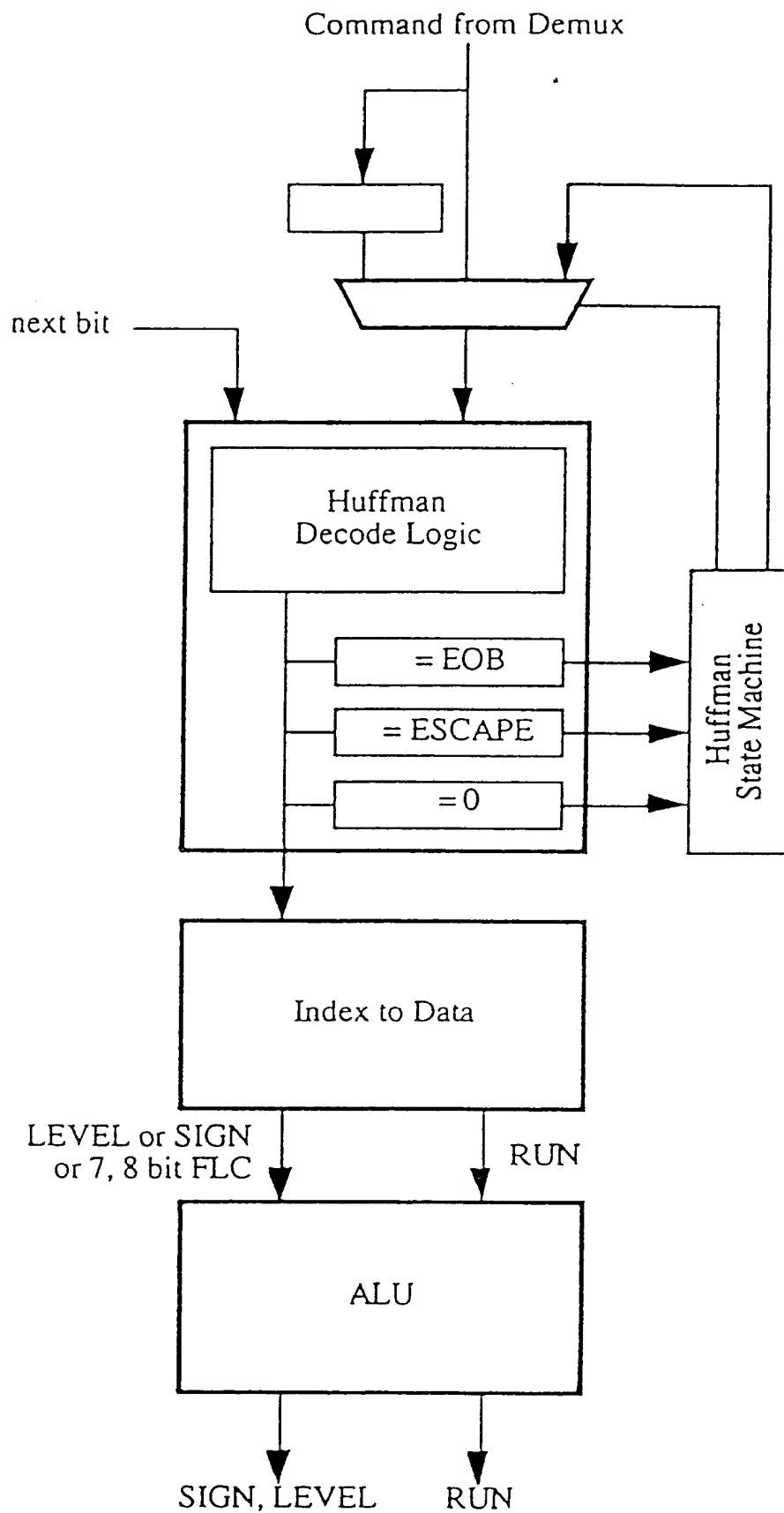


FIG. 124

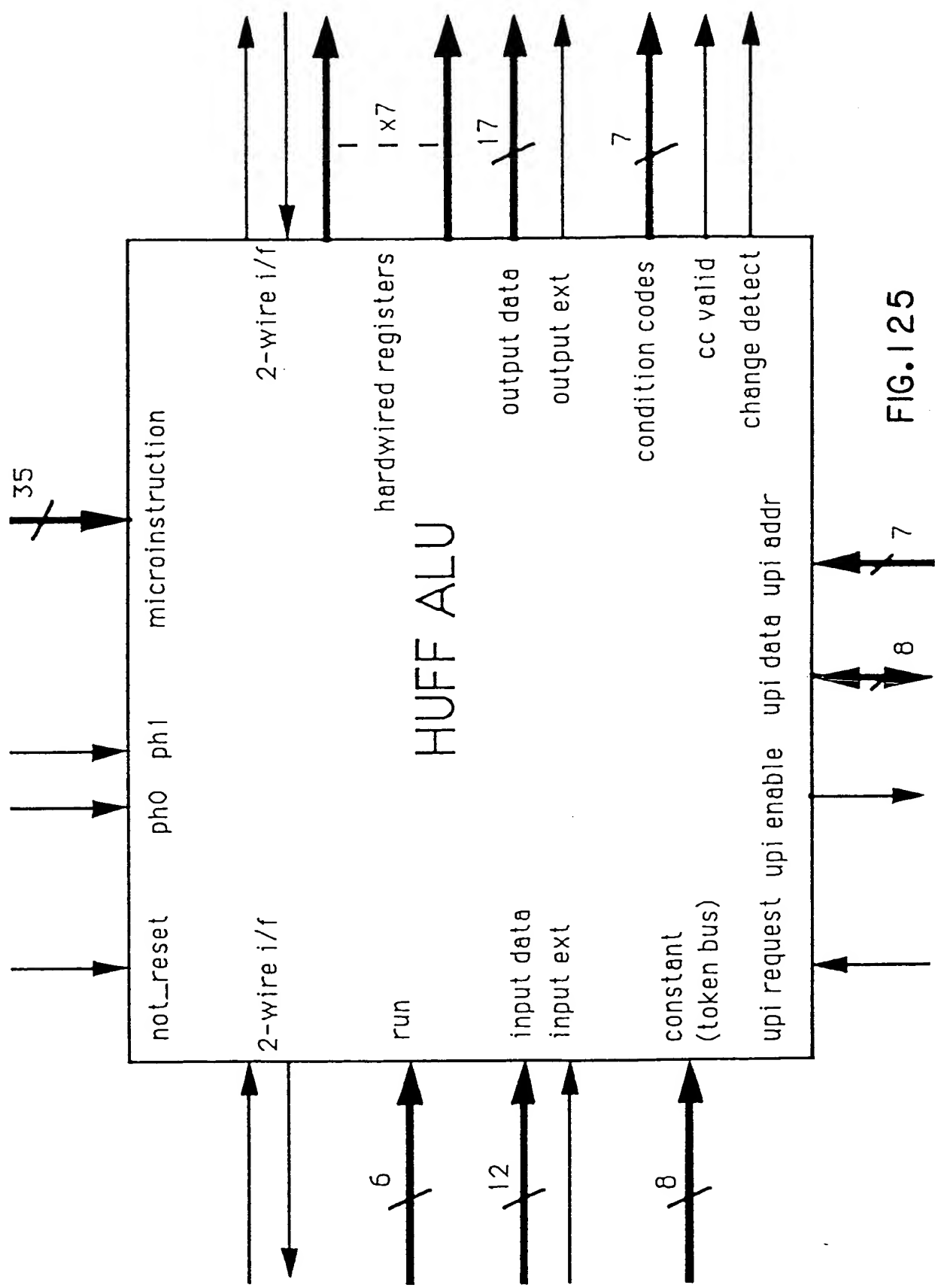


FIG. 125

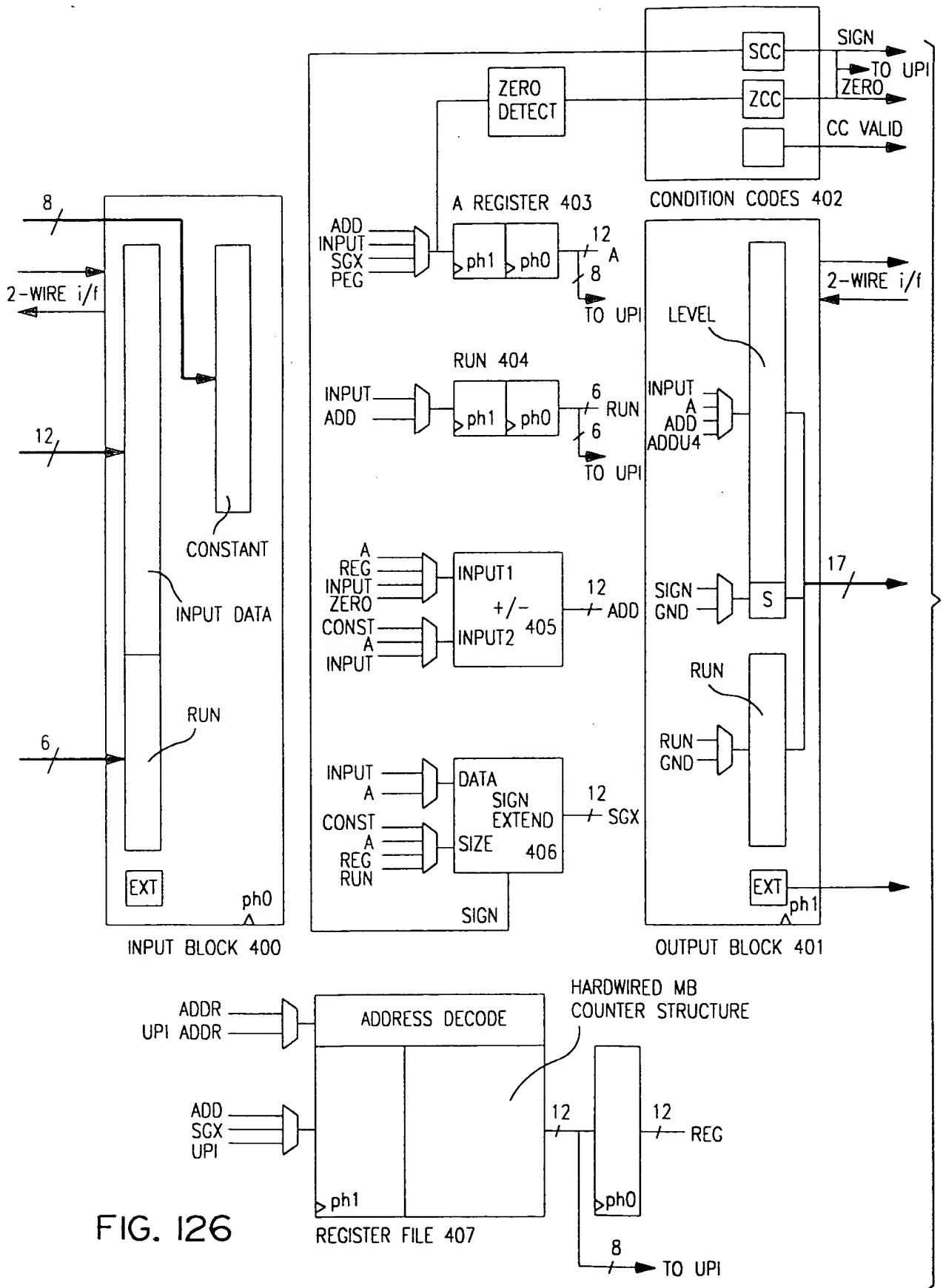


FIG. 126

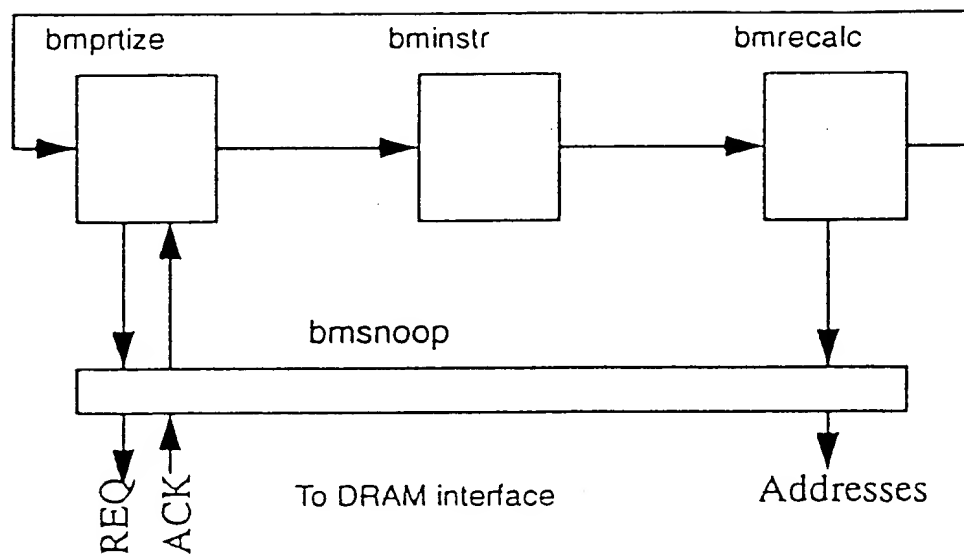


FIG. 127

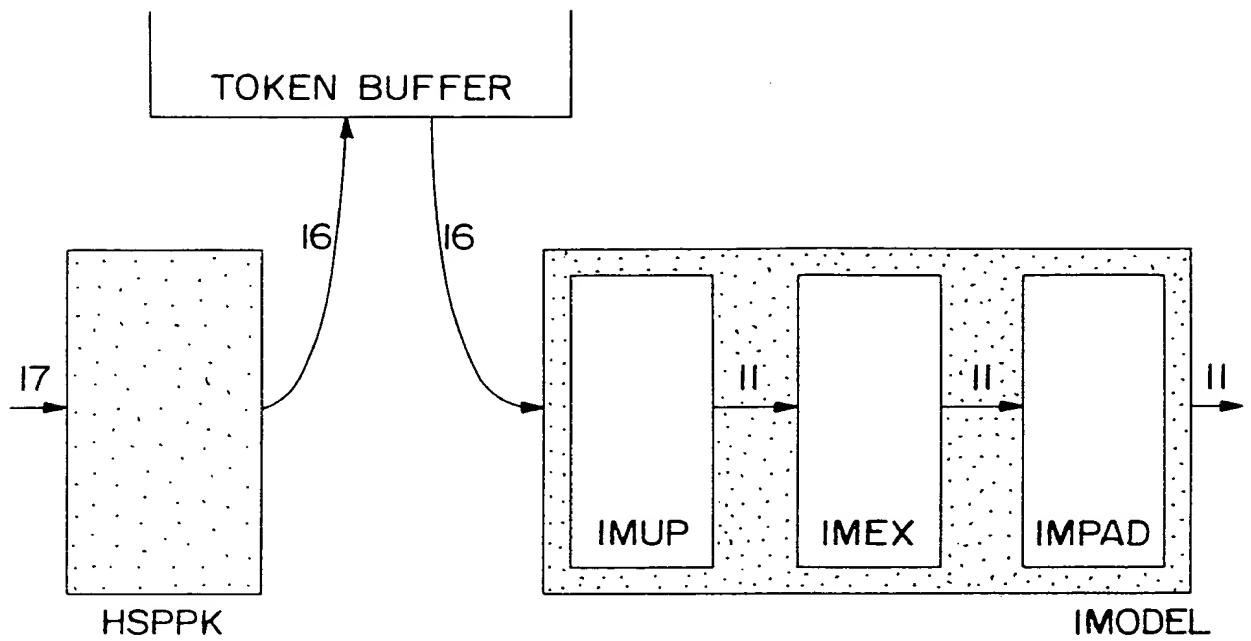


FIG. 128

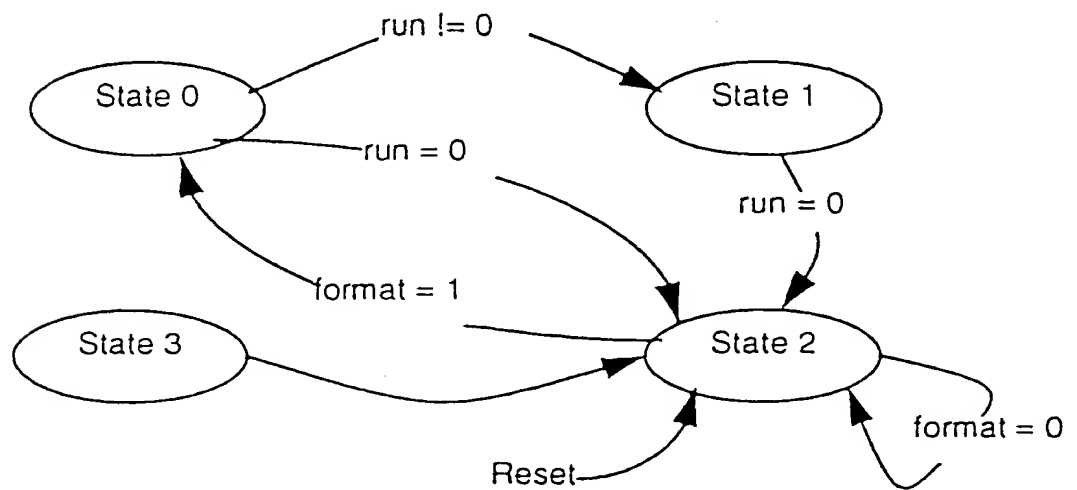


FIG. 129

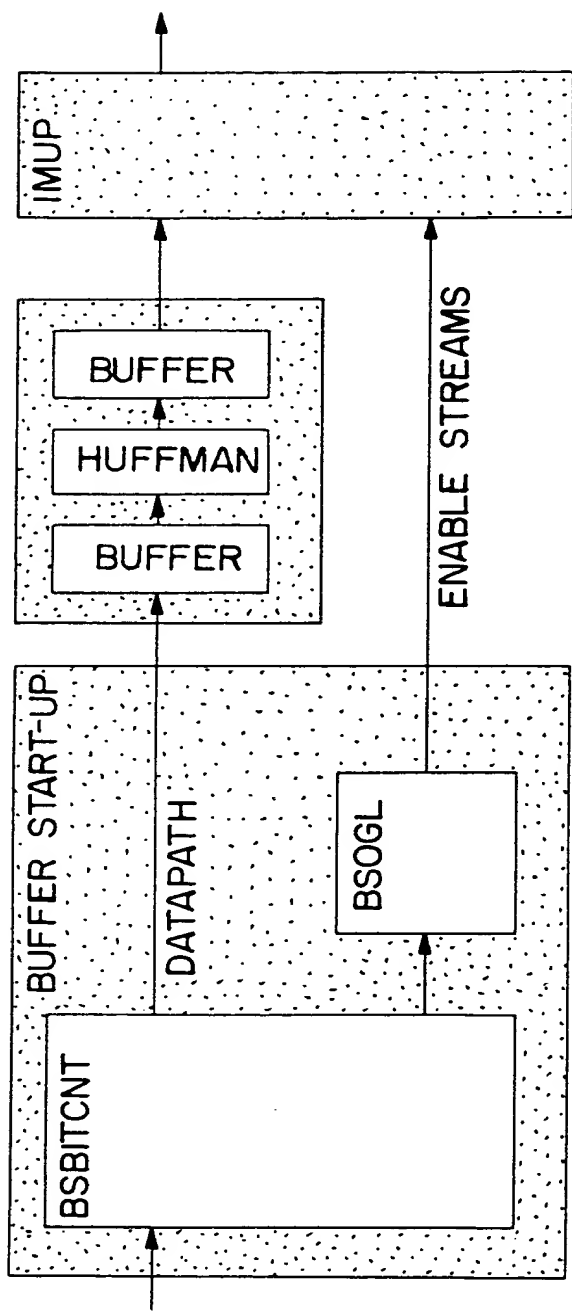


FIG. 130

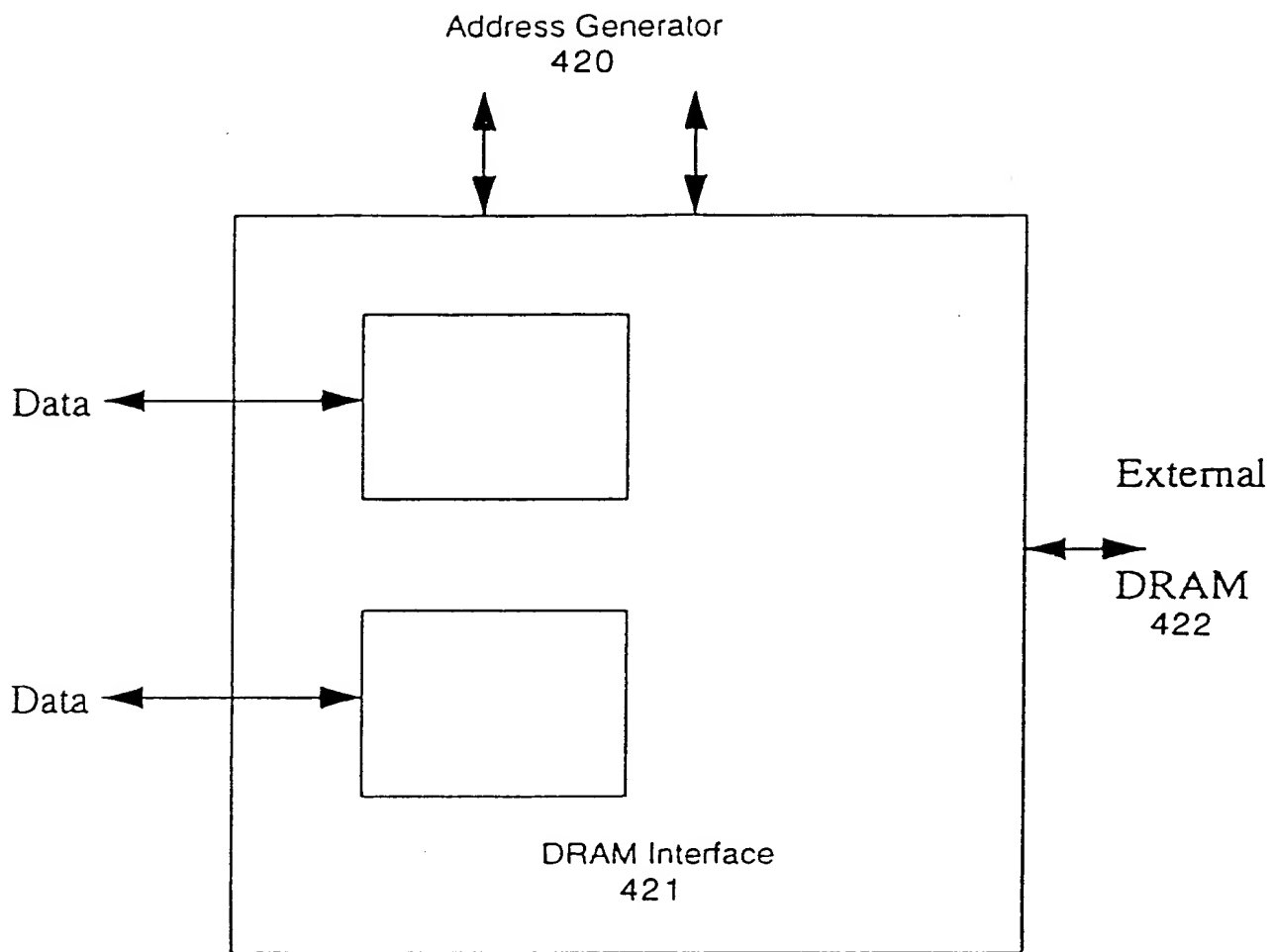


FIG. 131

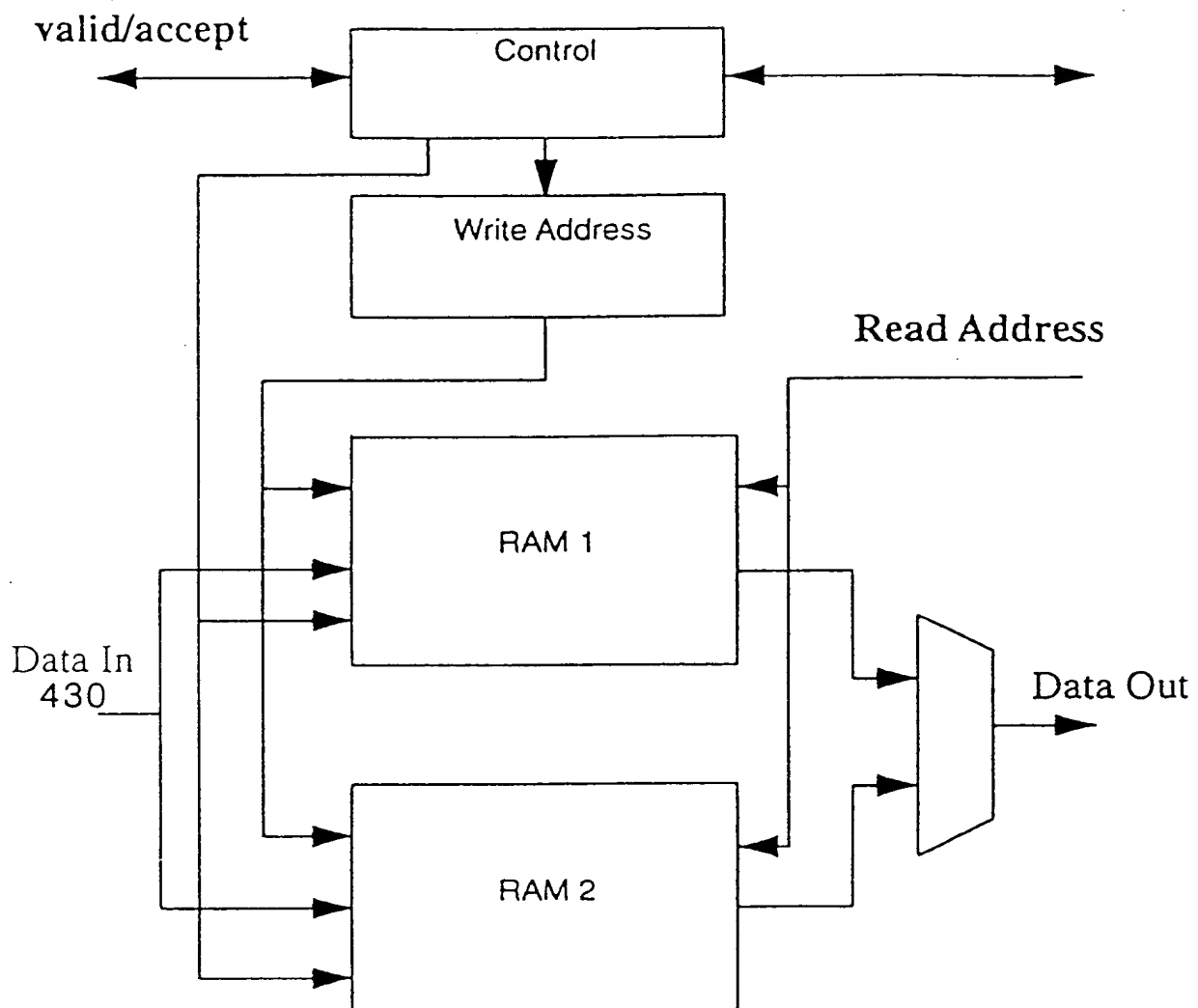


FIG. 132

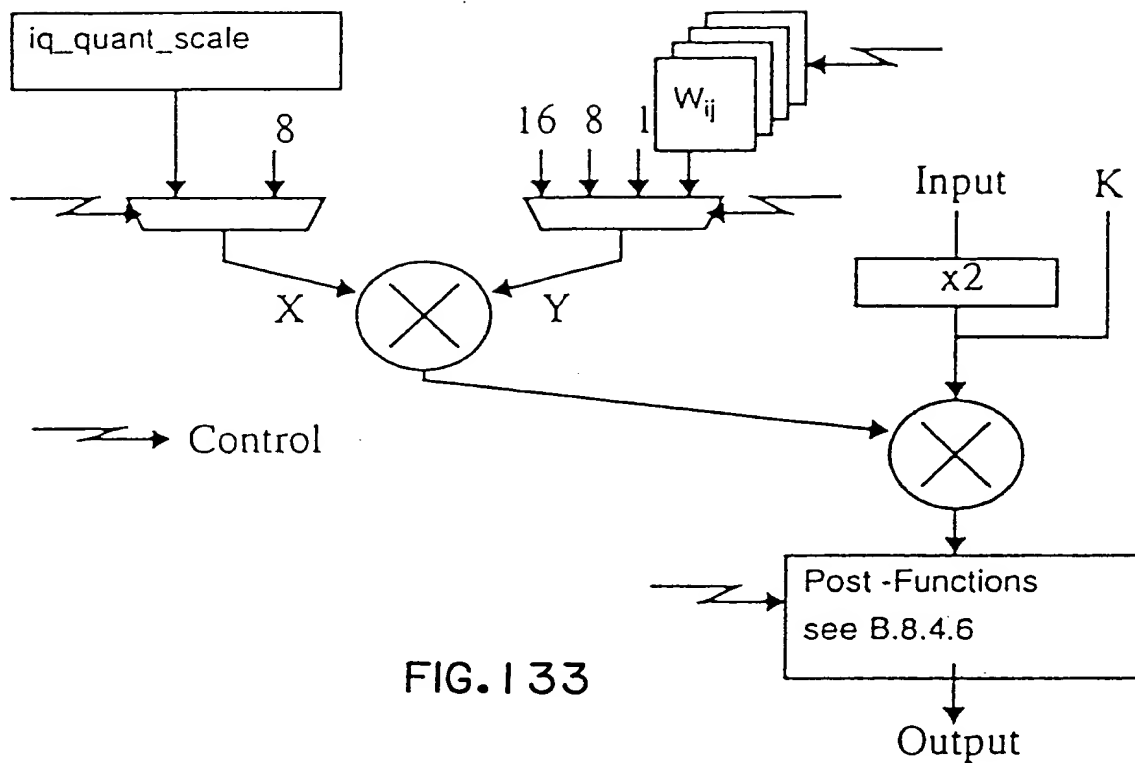


FIG. 133

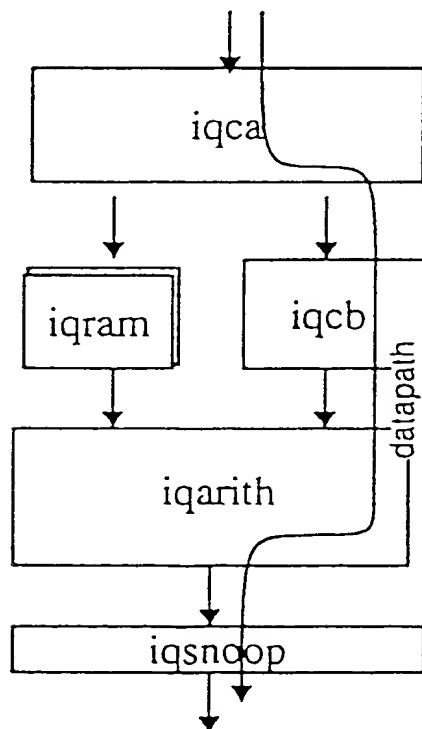


FIG. 134

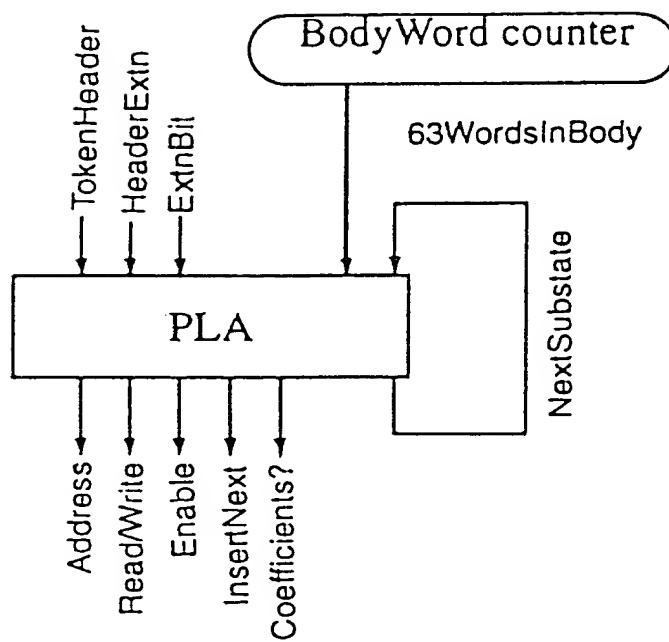


FIG. 135

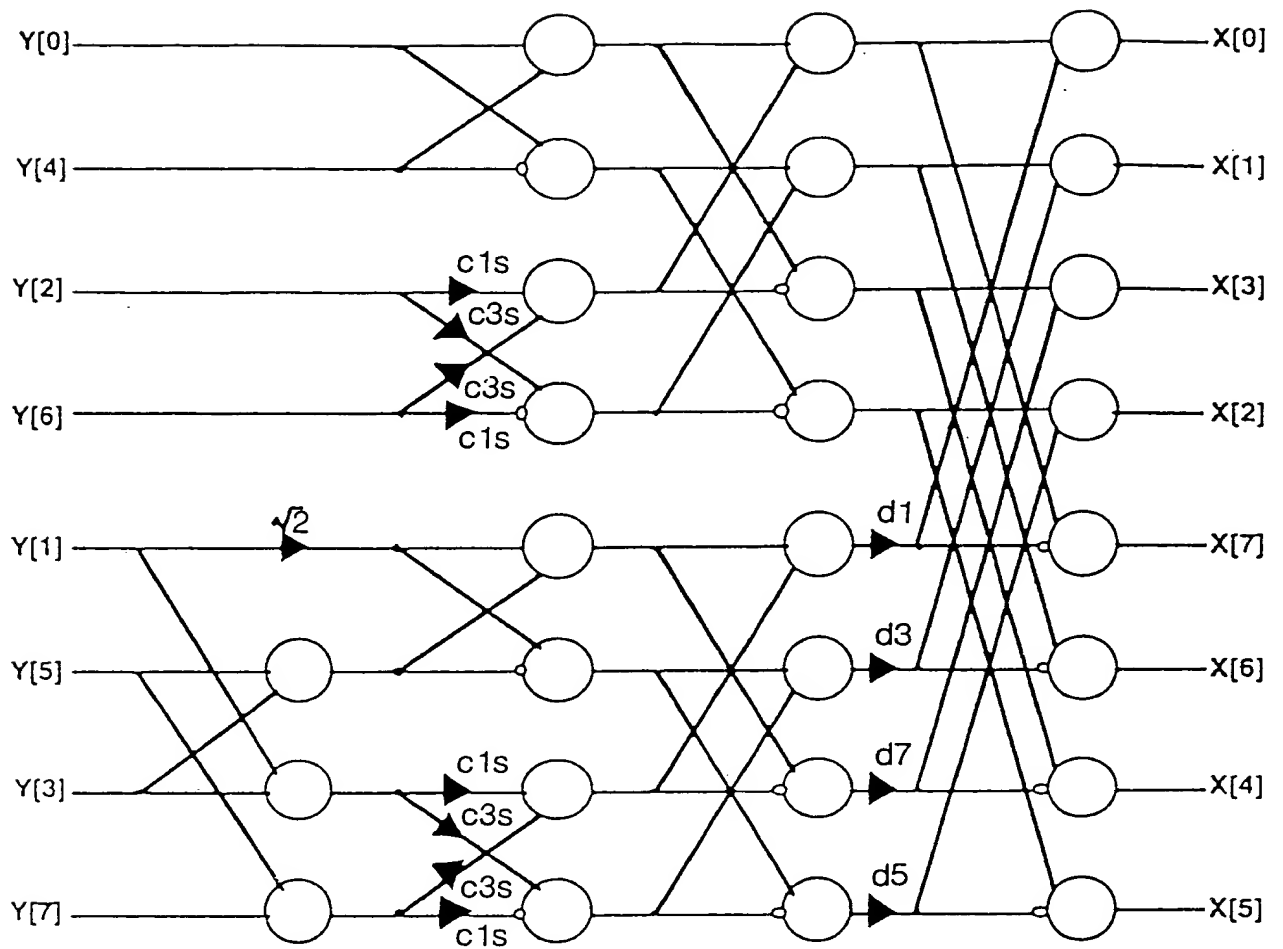
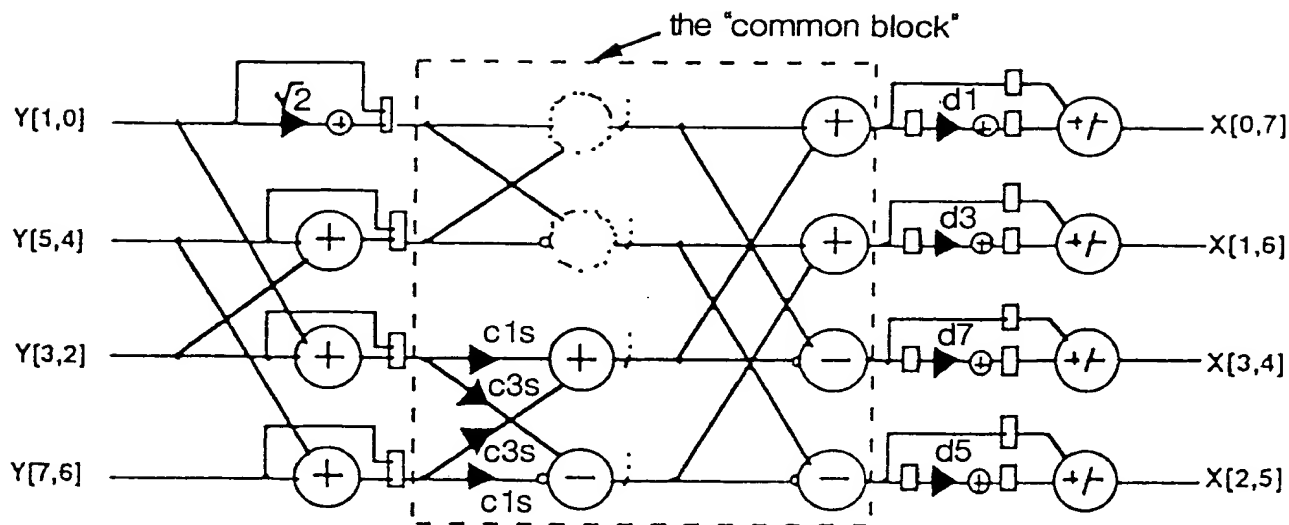


FIG. 136



Key:

coef constant coefficient
 ➤ carry-save multiplier
 ⊕ multiplier output resolver
 ⊕, ⊖ resolving adder, subtractor
 ⊕, ⊖ resolving adder/subtractor

⊕, ⊖ carry-save adder, subtractor
 ⊕, ⊖ dummy adder/subtractor (combiners)
 □ latch
 □ 2-input mux latch

FIG. 137

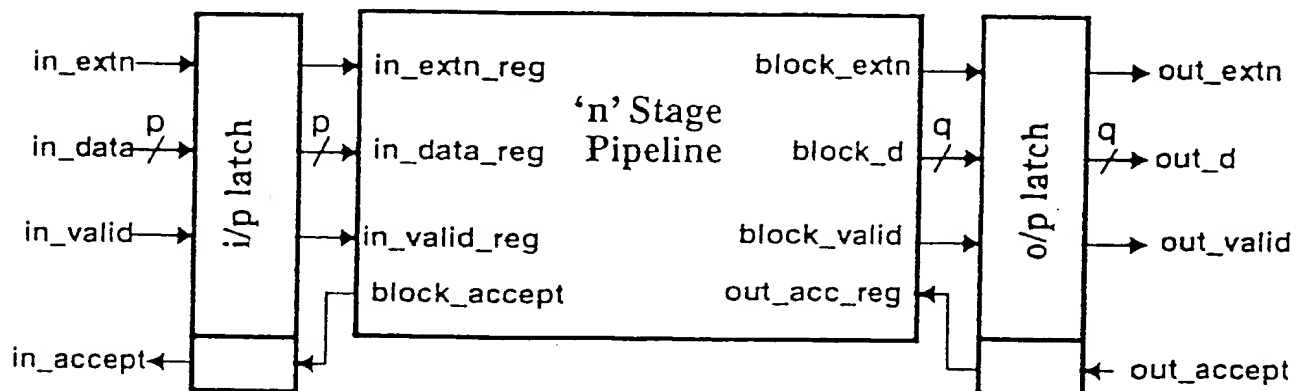


FIG. 138

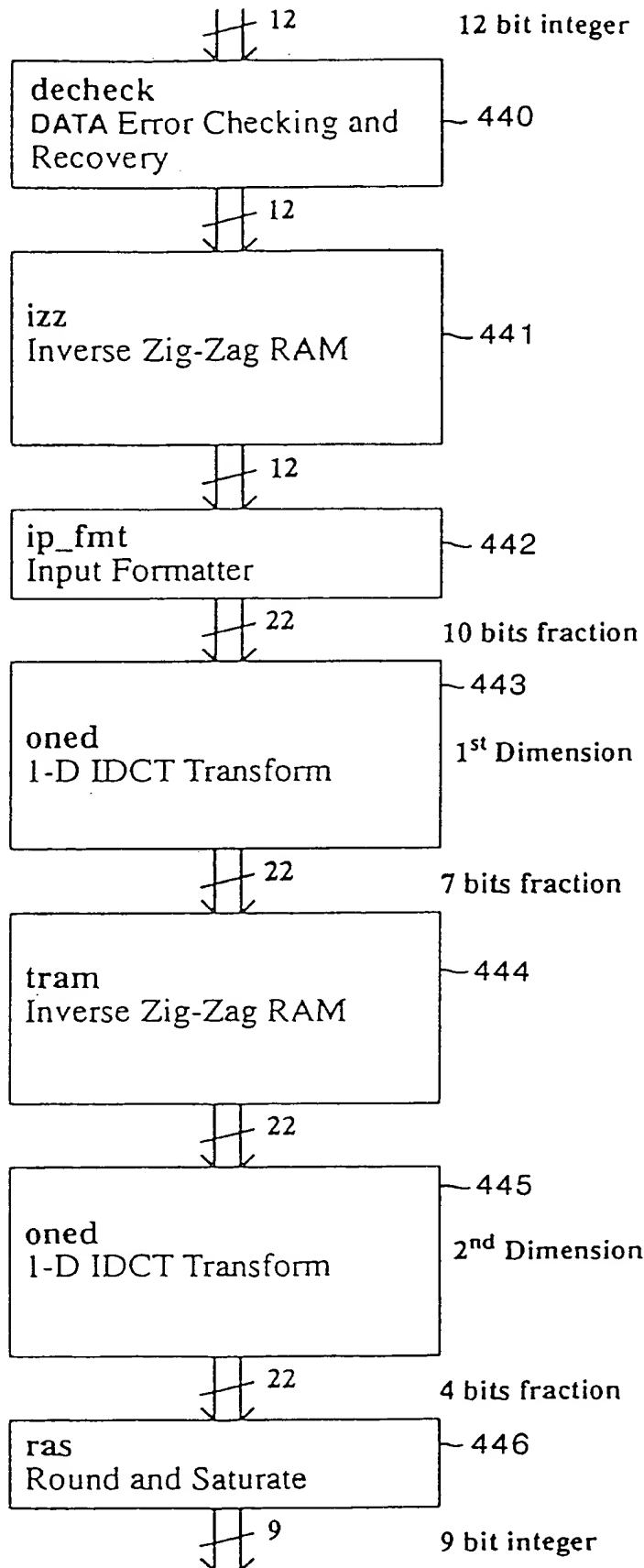


FIG. 139

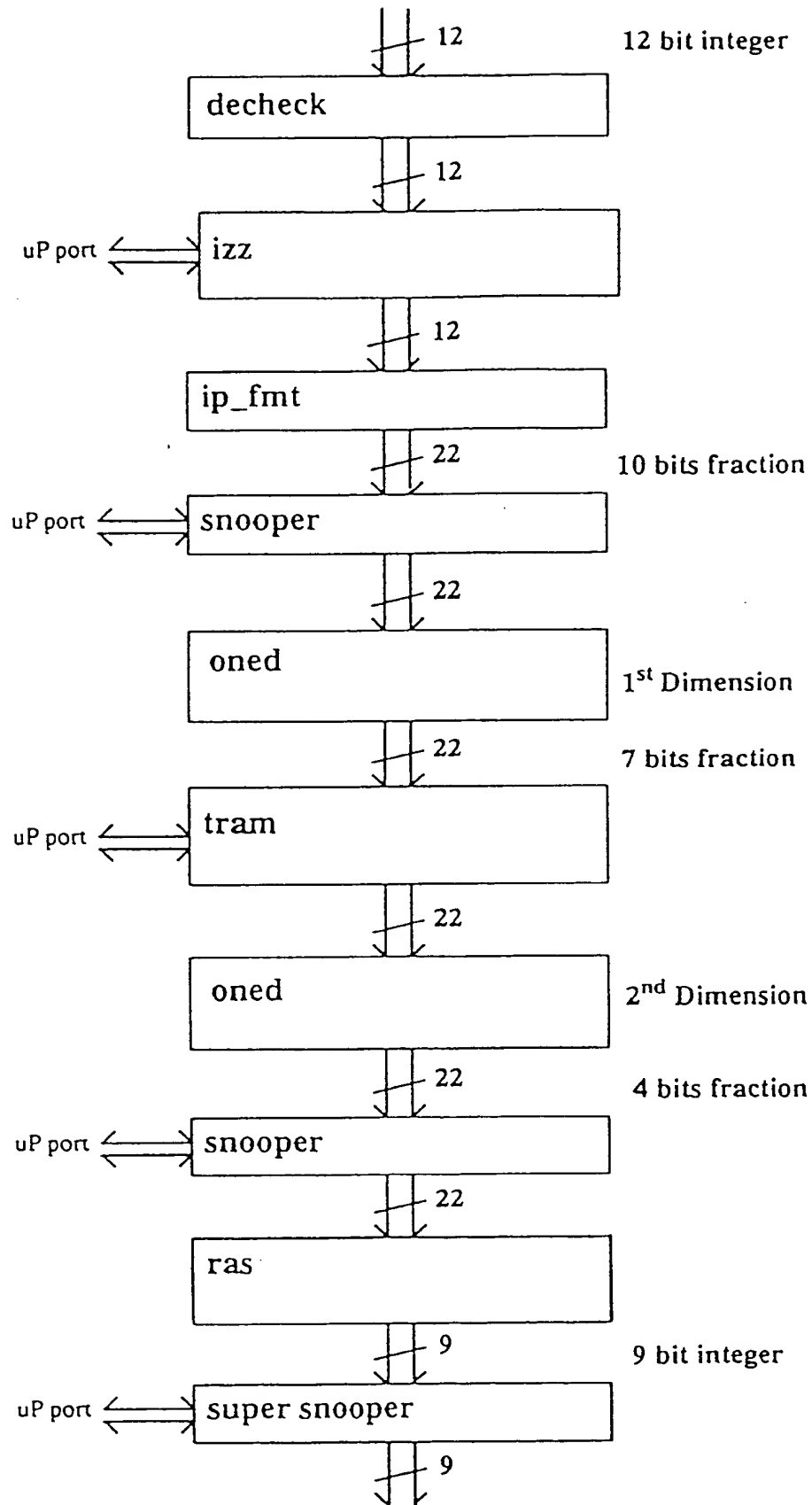
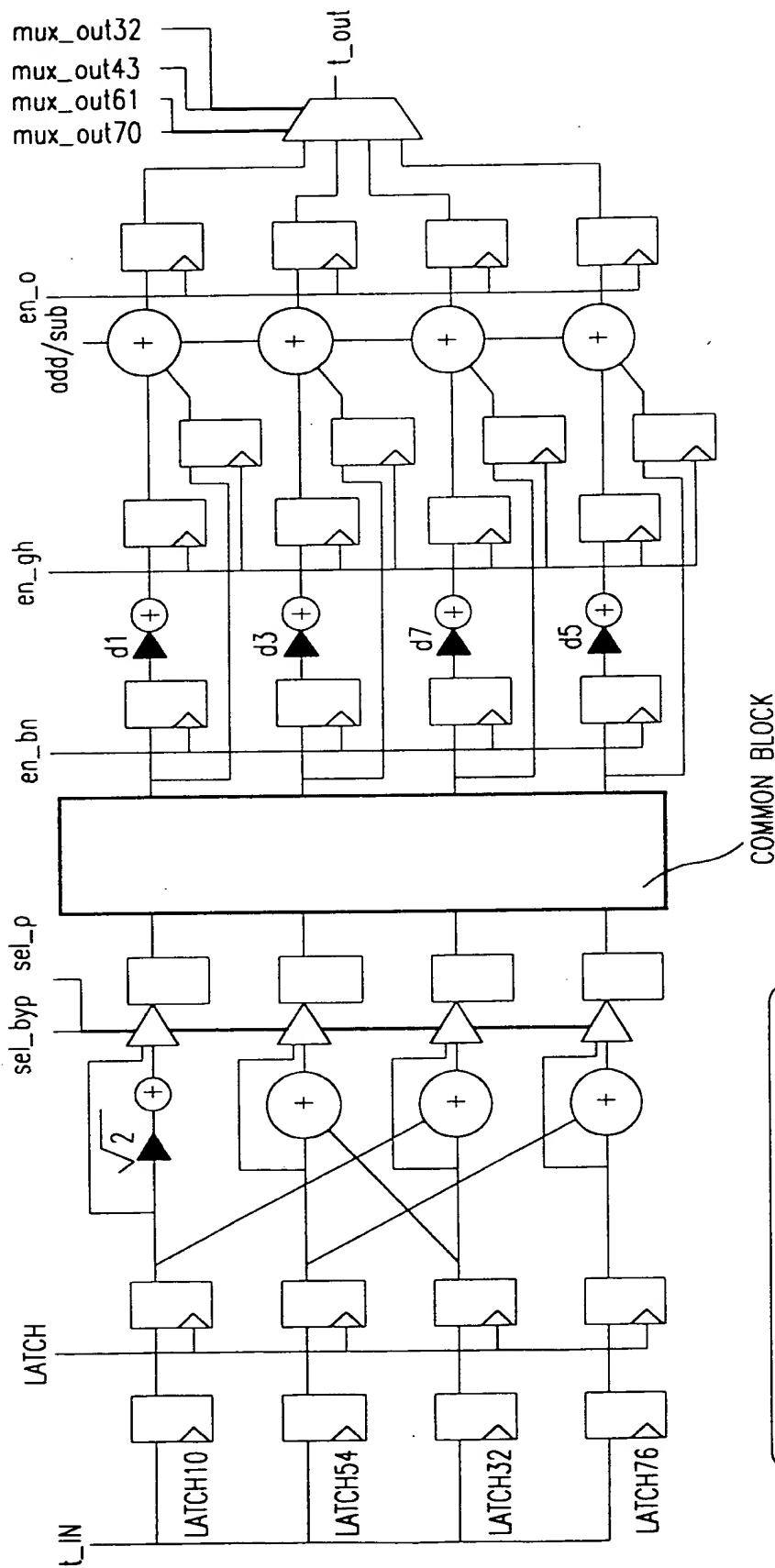


FIG. 140



NOTE: "COMMON BLOCK" IS ENTIRELY COMBINATIONAL (NO LATCHING)

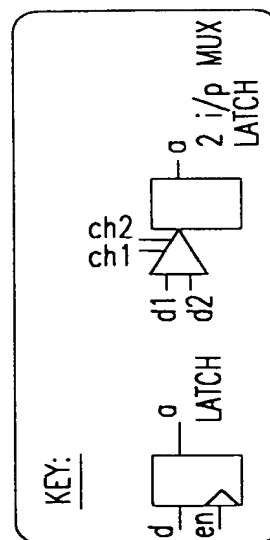


FIG. 141

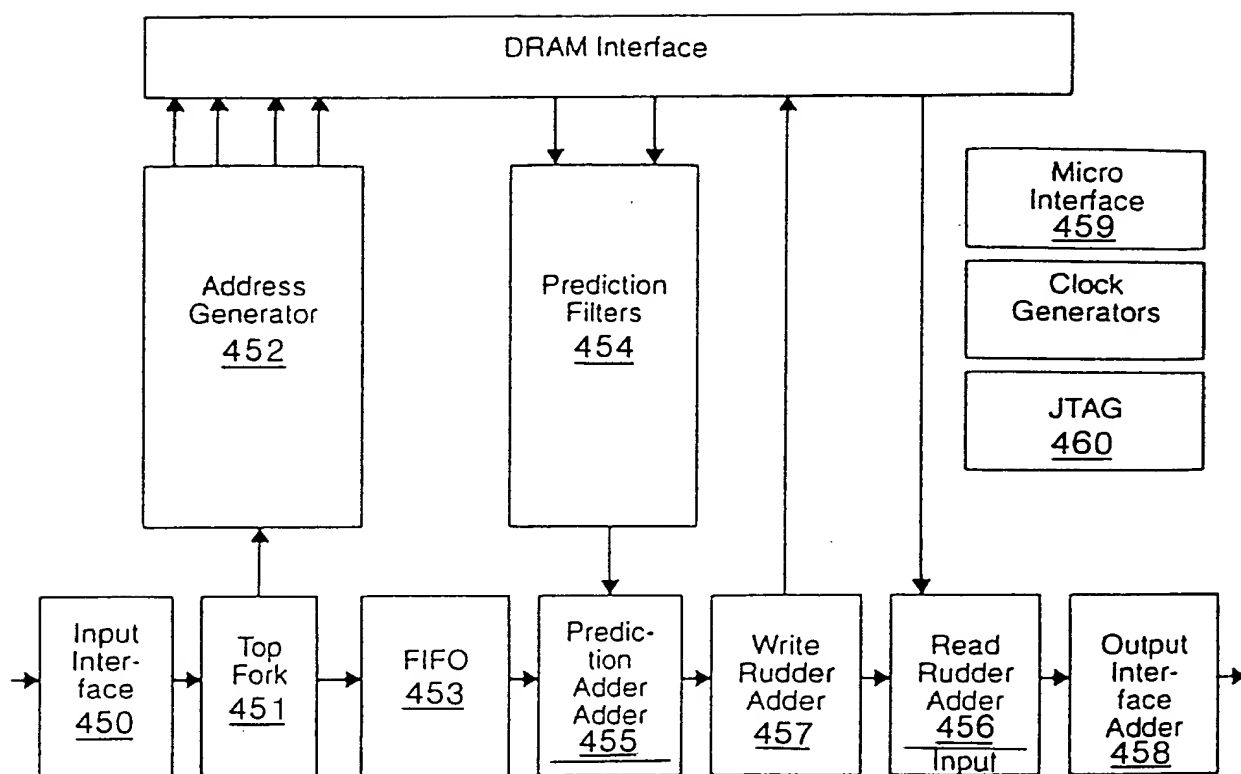


FIG. 142

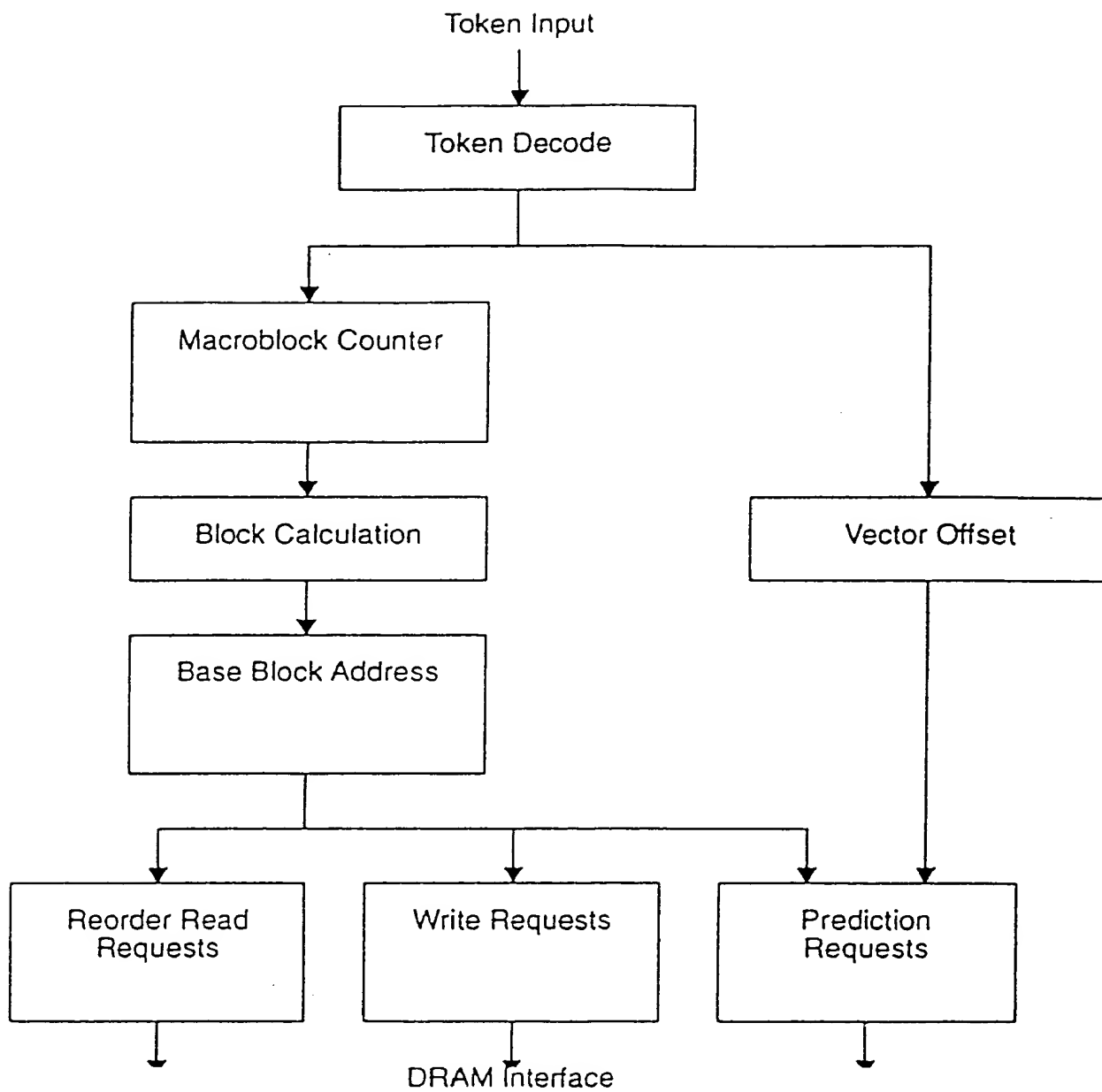


FIG. 144

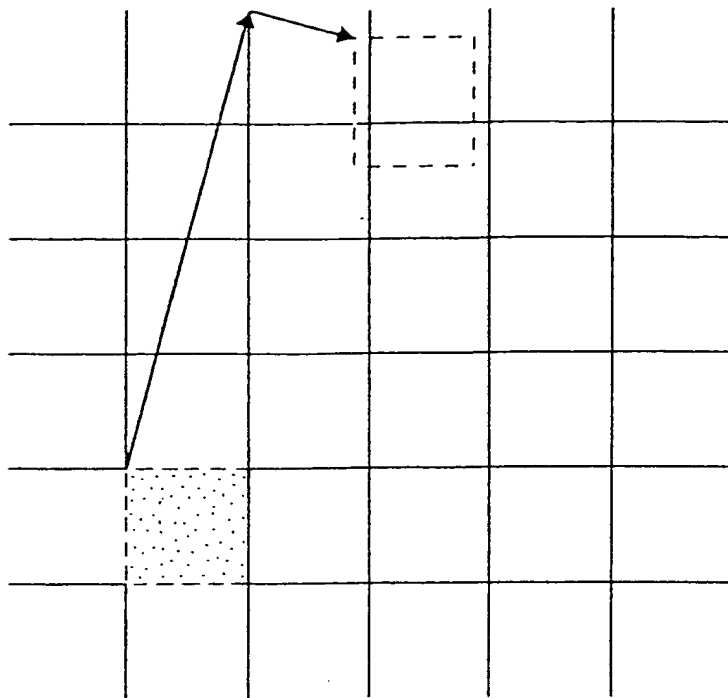


FIG. 1 45

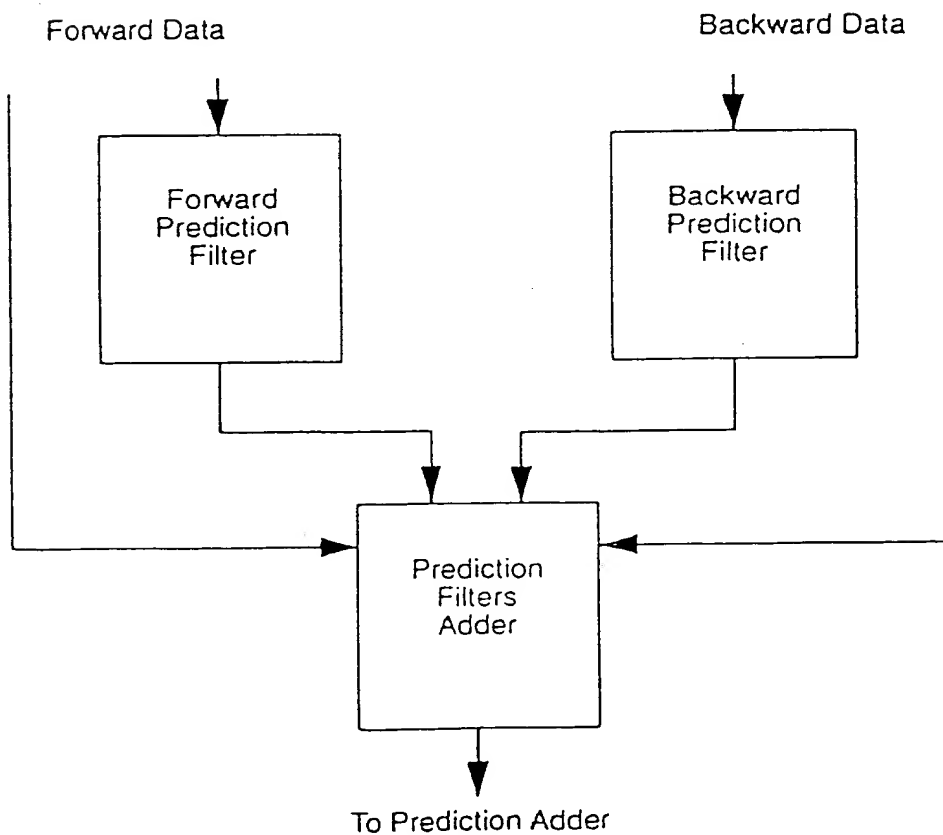


FIG. 1 46

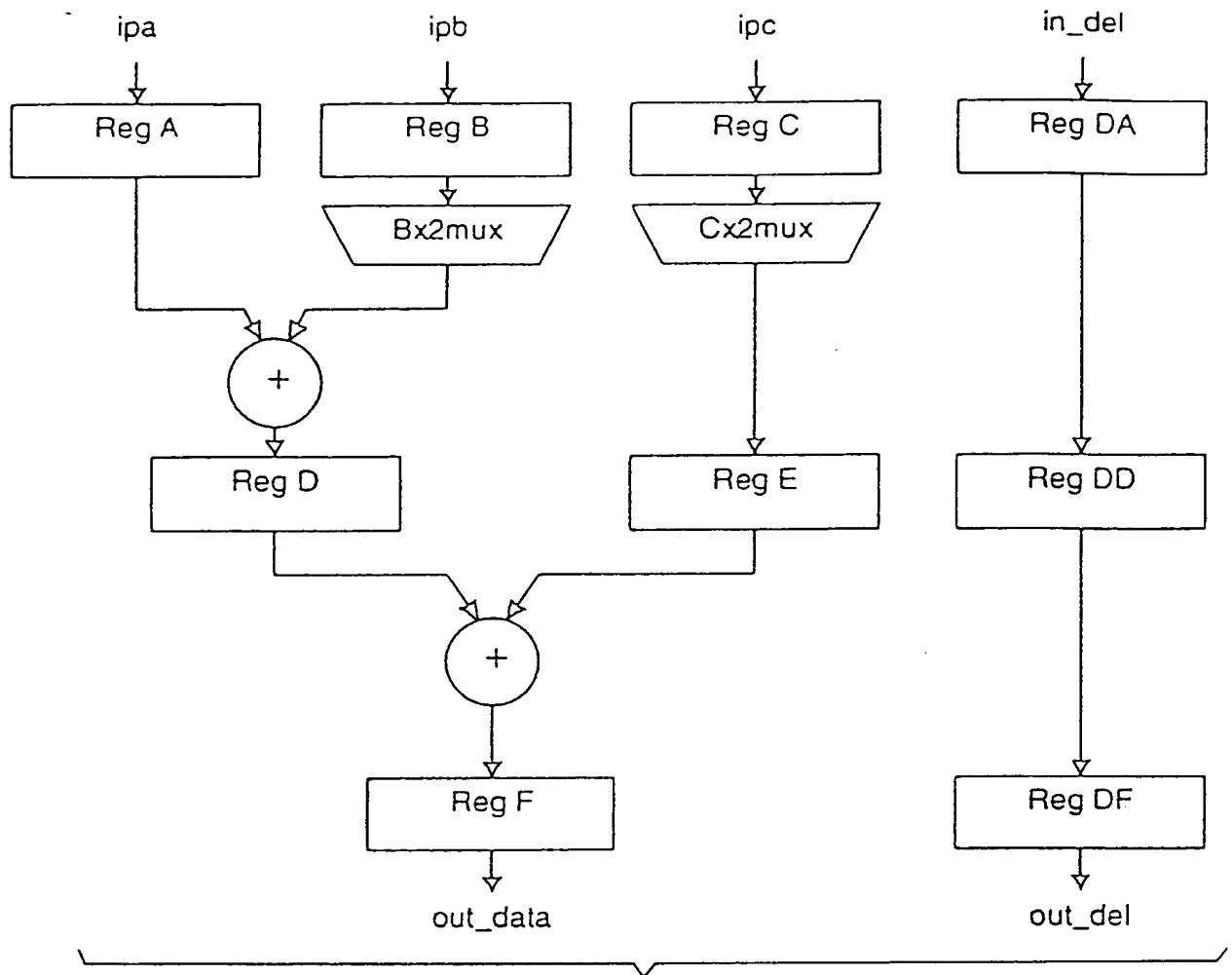


FIG. 148

0	1	2	3	4	5	6	7
8	9	10	11	12	13	14	15
16	17	18	19	20	21	22	23
24	25	26	27	28	29	30	31
32	33	34	35	36	37	38	39
40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55
56	57	58	59	60	61	62	63

FIG. 149

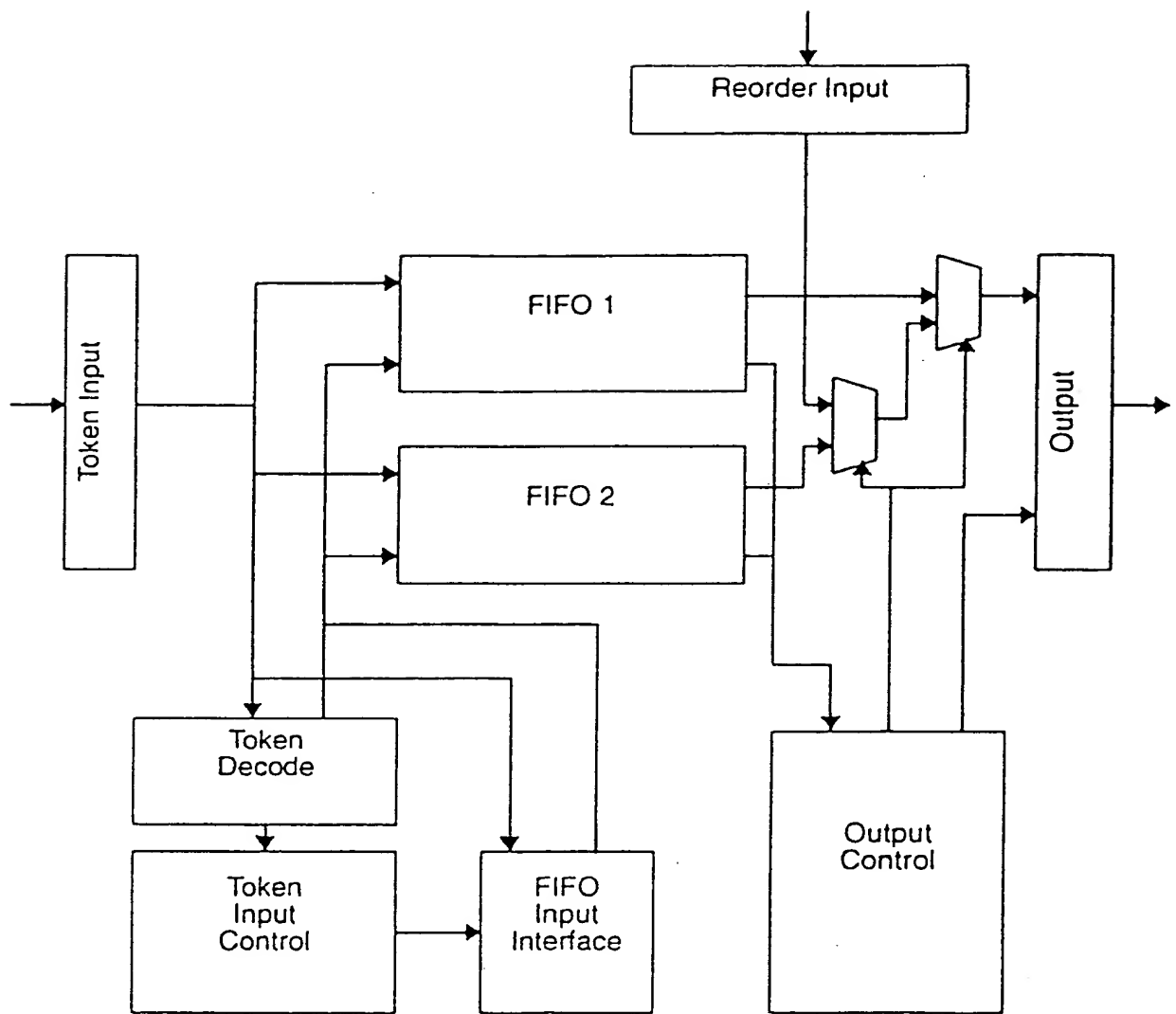


FIG. 150

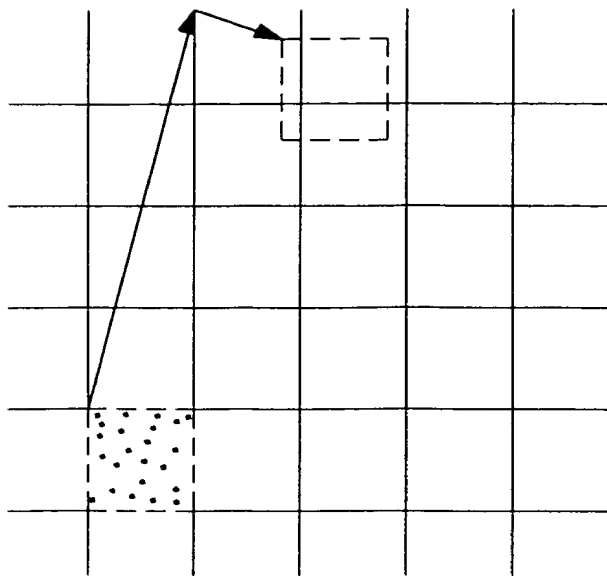


FIG. 151

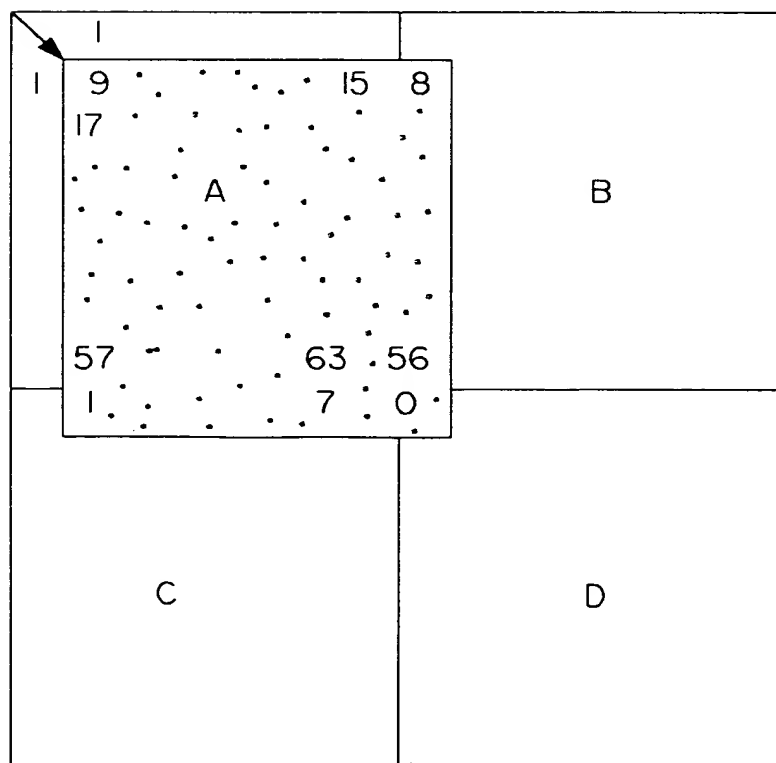


FIG. 152

Read Cycle

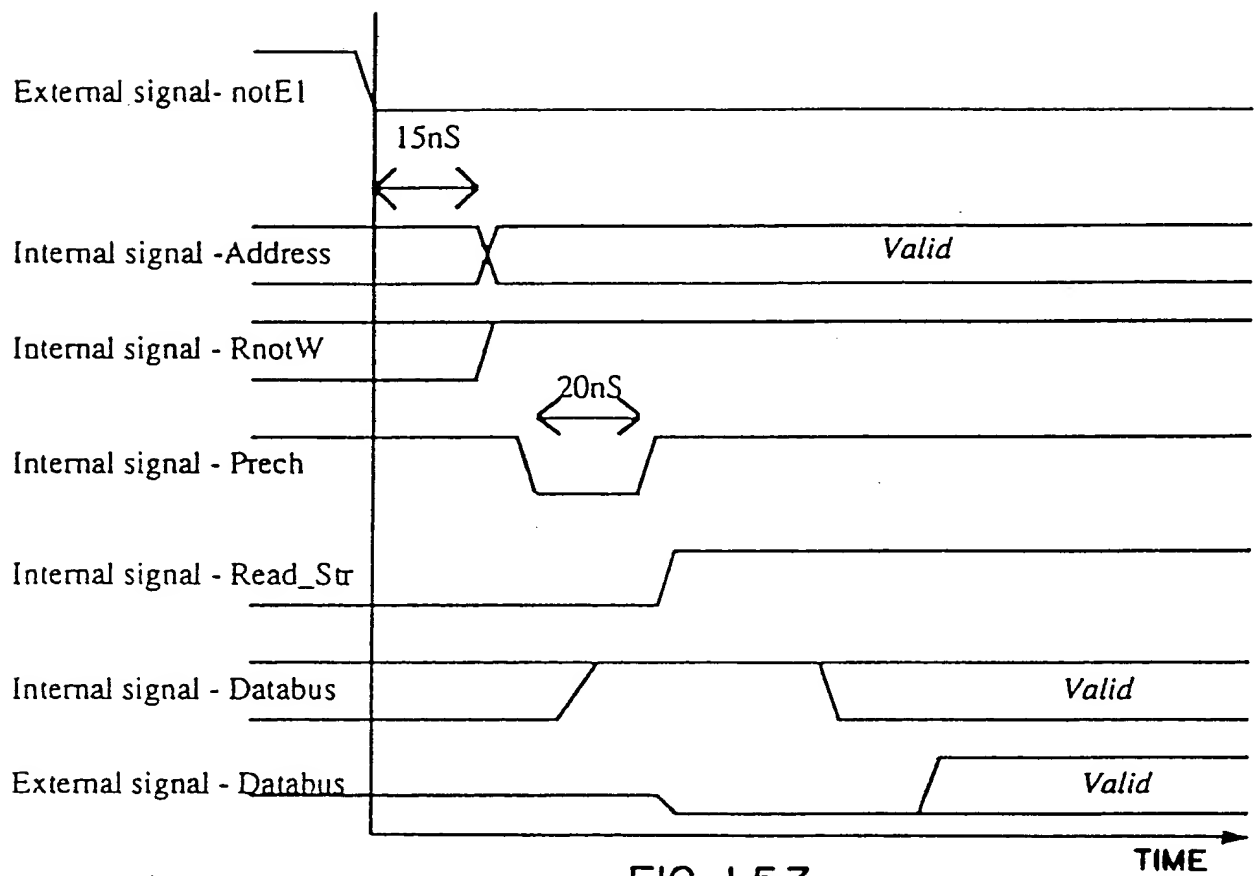


FIG. 153

Write Cycle

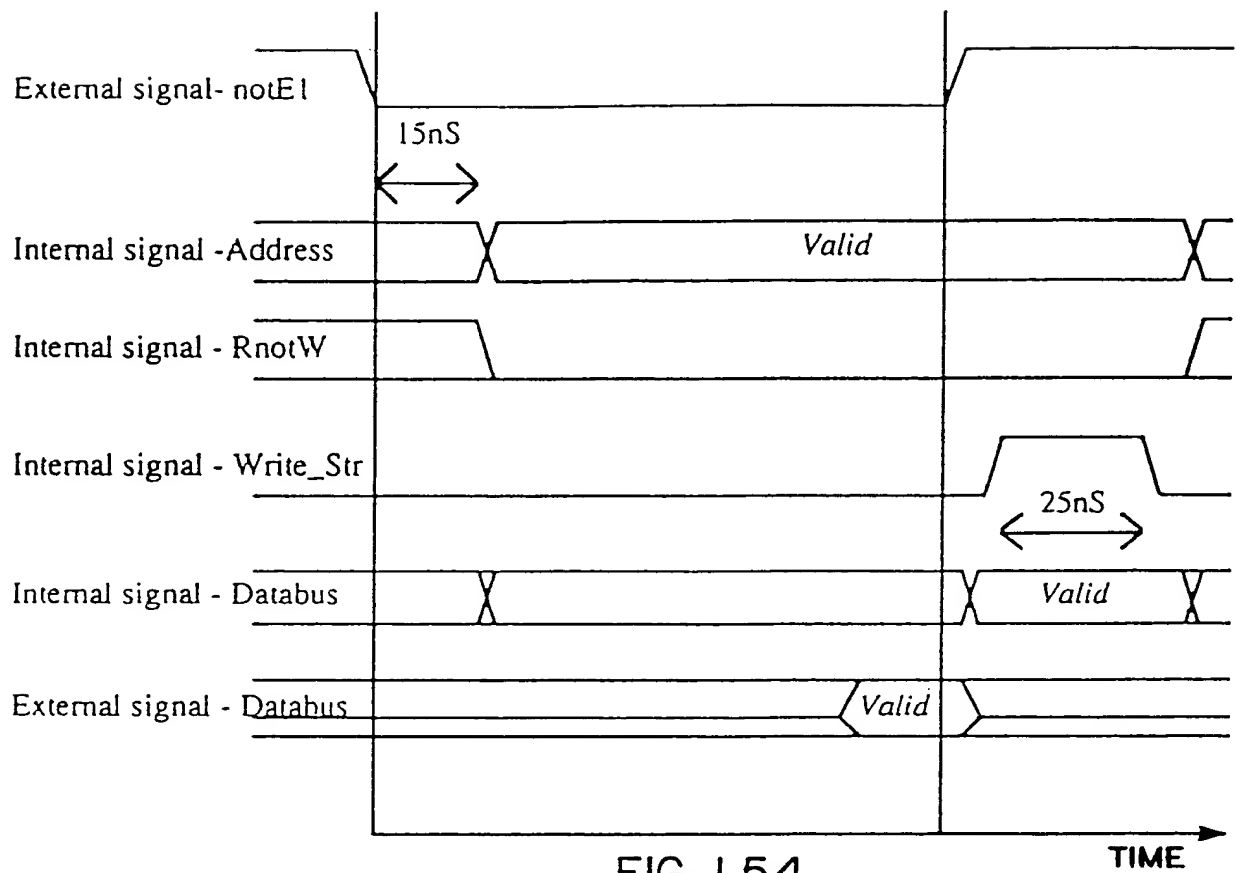


FIG. 154

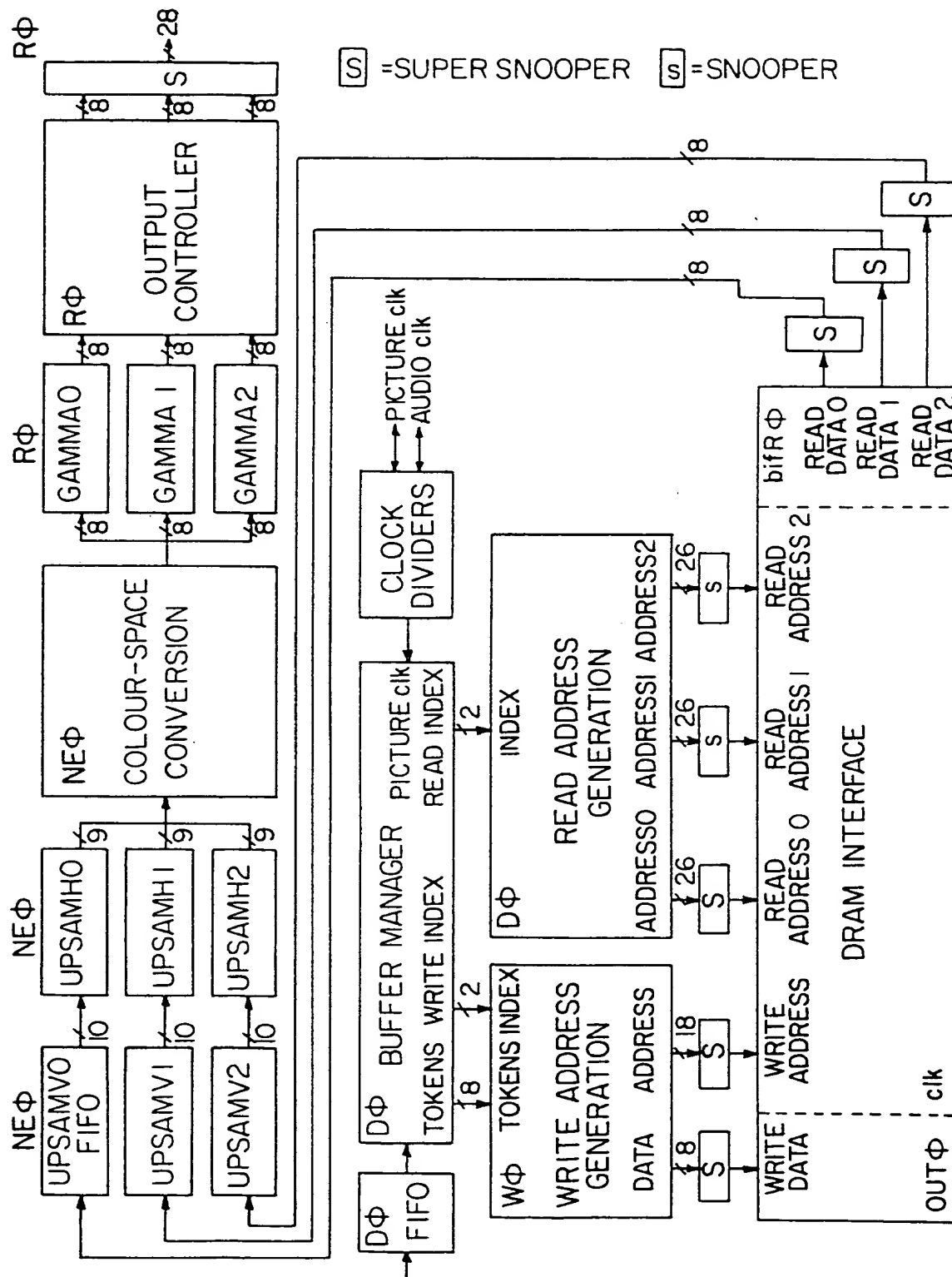


FIG. 155

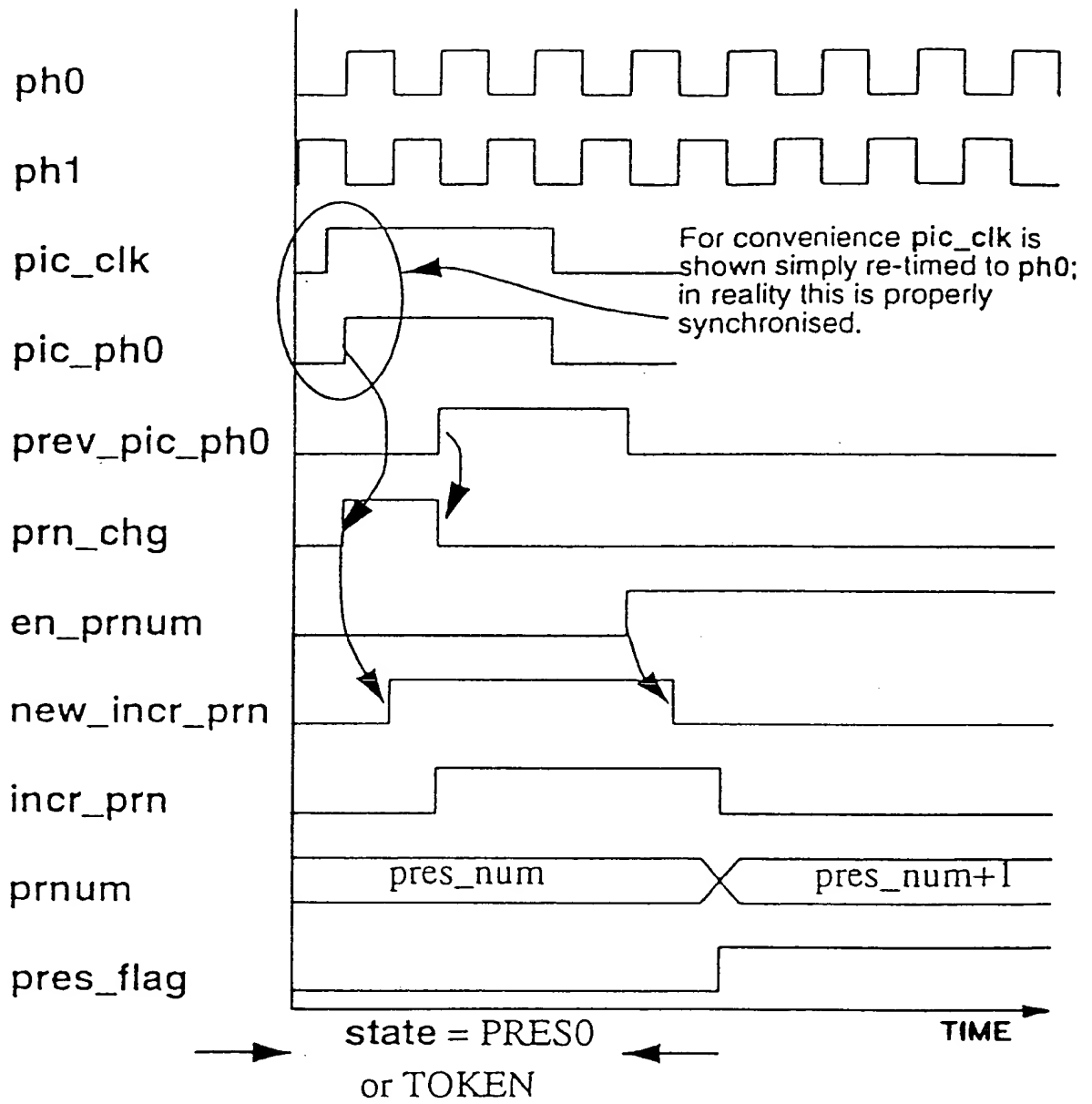


FIG. 156

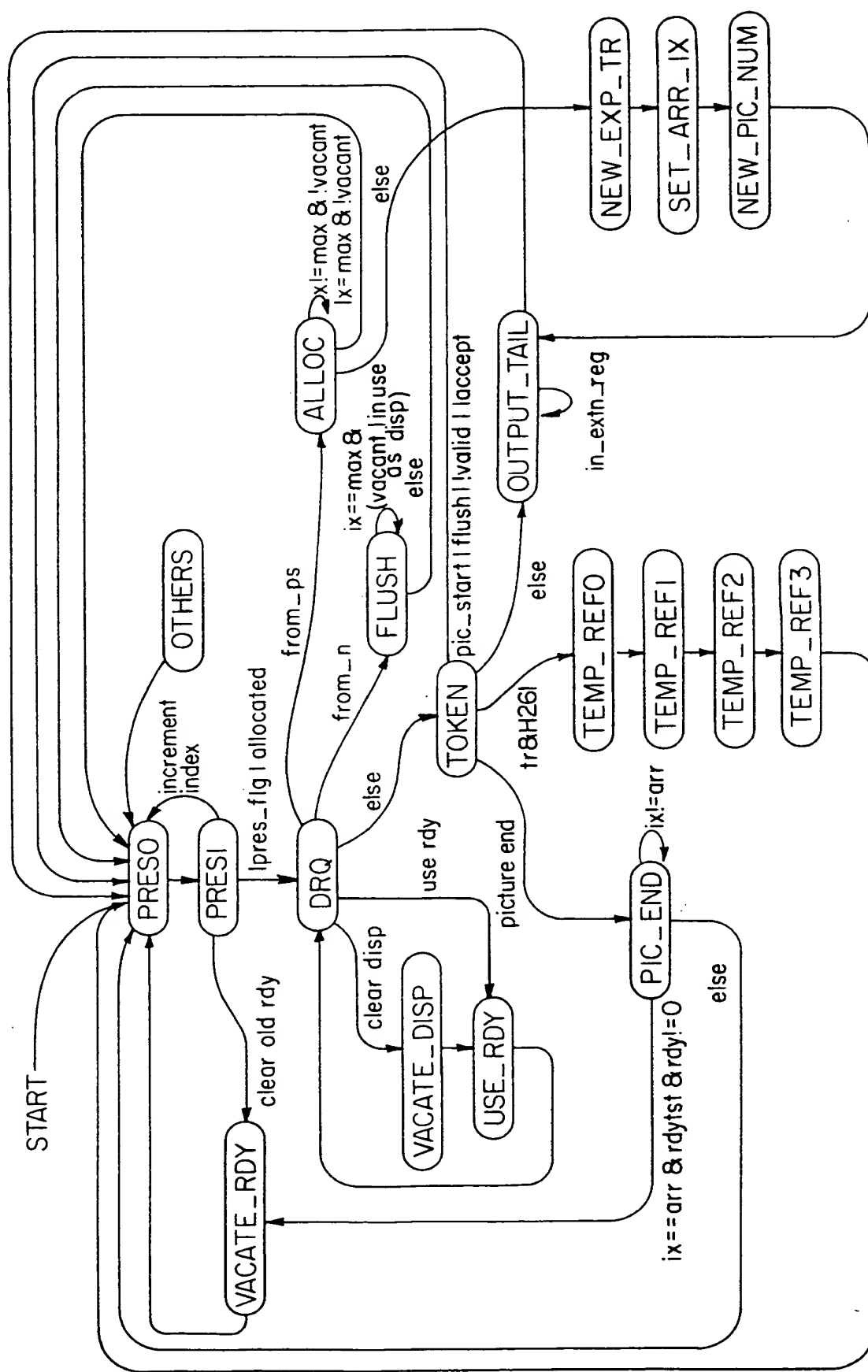


FIG. 157

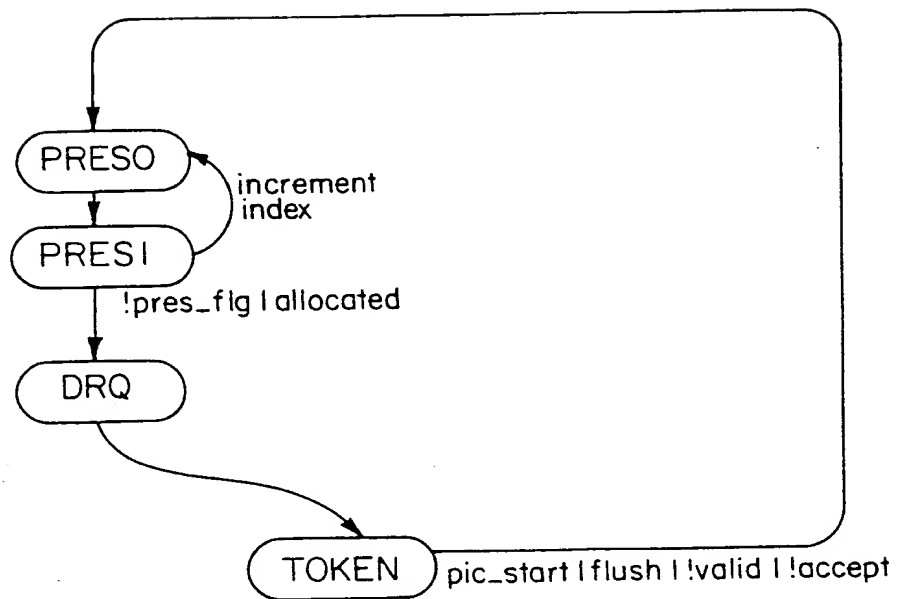


FIG. 158

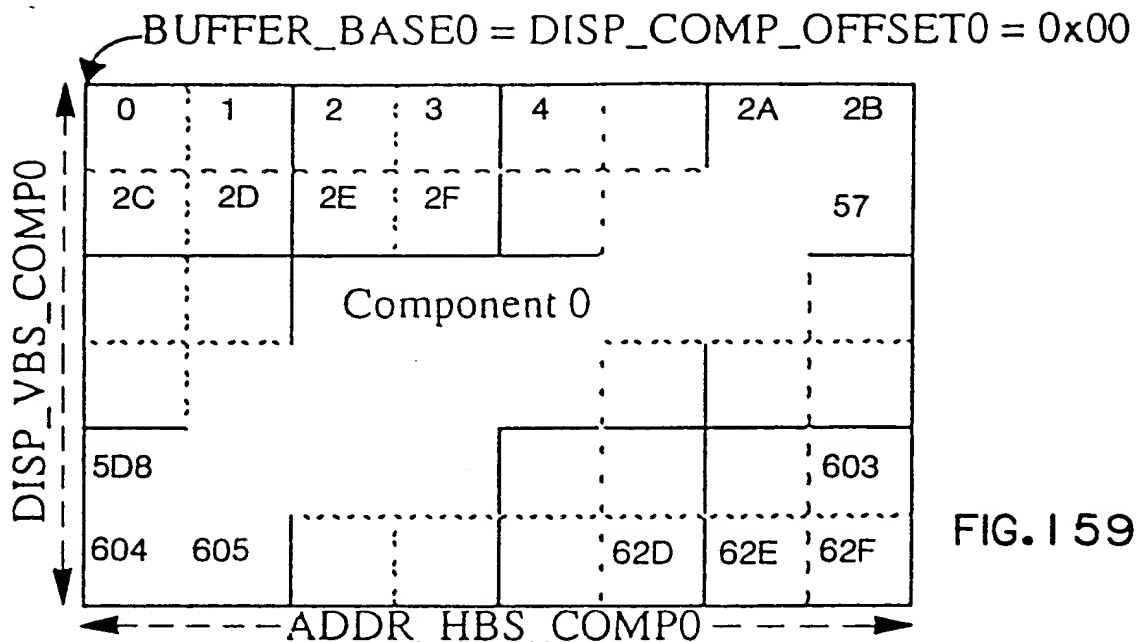


FIG. 1 59A

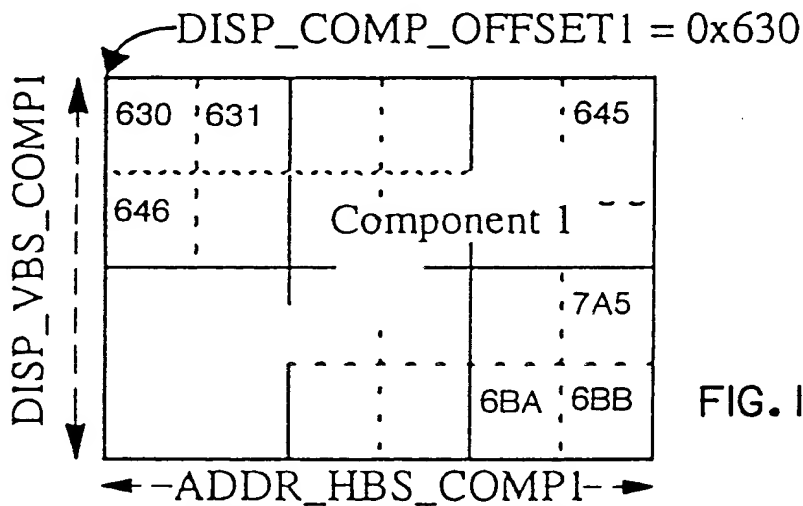


FIG. 1 59B

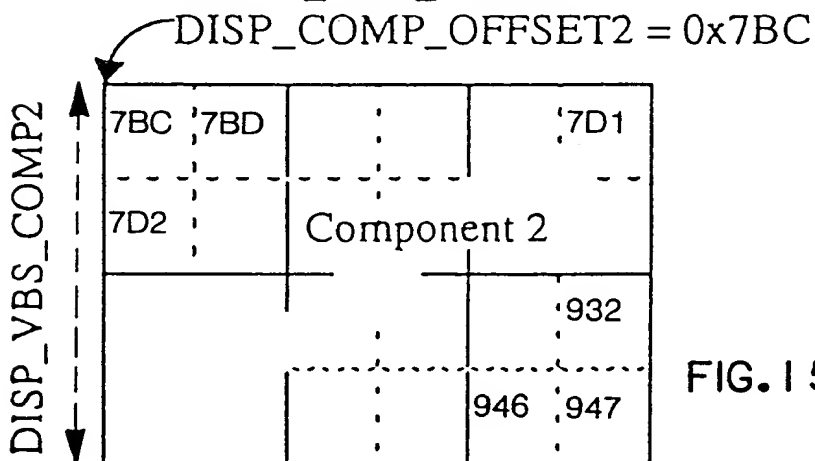


FIG. 1 59C

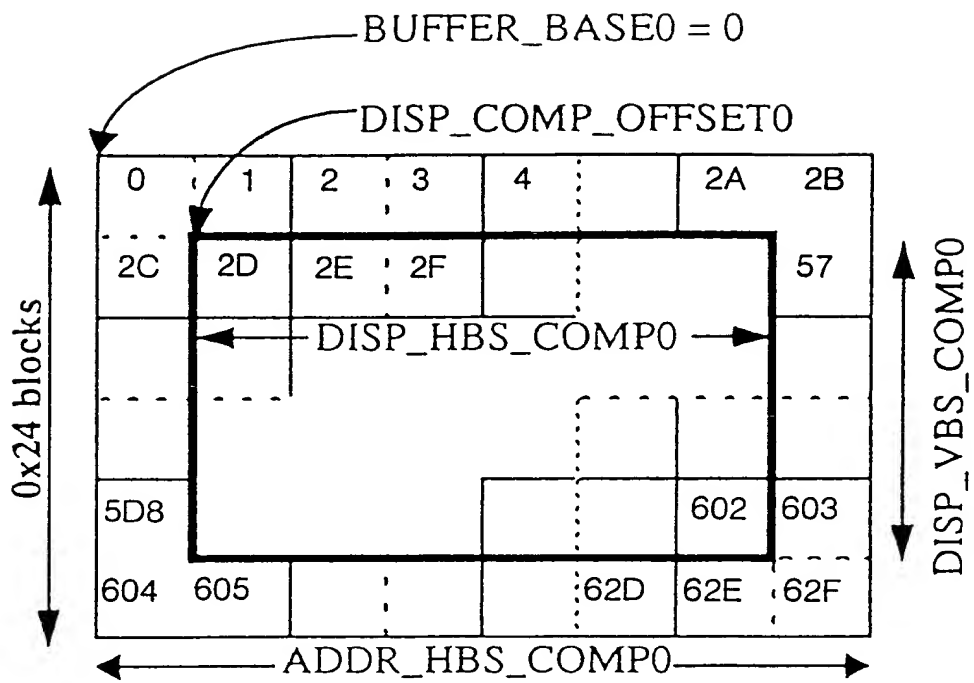


FIG. 160

BUFFER OFFSET 0x00

COMPONENT OFFSET 0x000 +

00	01	02	03	04	05	06	07	08	09	0A	0B
0C	0D	0E	0F	10	11	12	13	14	15	16	17
18	19	1A	1B	1C	1D	1E	1F	20	21	22	23
24	25	26	27	28	29	2A	2B	2C	2D	2E	2F
30	31	32	33	34	35	36	37	38	39	3A	3B
3C	3D	3E	3F	40	41	42	43	44	45	46	47
48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
60	61	62	63	64	65	66	67	68	69	6A	6B
6C	6D	6E	6F	70	71	72	73	74	75	76	77
78	79	7A	7B	7C	7D	7E	7F	80	81	82	83
84	85	86	87	88	89	8A	8B	8C	8D	8E	8F

FIG. 161A

COMPONENT1 OFFSET 0x100 +

00	01	02	03	04	05
06	07	08	09	0A	0B
0C	0D	0E	0F	10	11
12	13	14	15	16	17
18	19	1A	1B	1C	1D
1E	1F	20	21	22	23

FIG. 161B

COMPONENT1 OFFSET 0x200 +

00	01	02	03	04	05
06	07	08	09	0A	0B
0C	0D	0E	0F	10	11
12	13	14	15	16	17
18	19	1A	1B	1C	1D
1E	1F	20	21	22	23

FIG. 161C

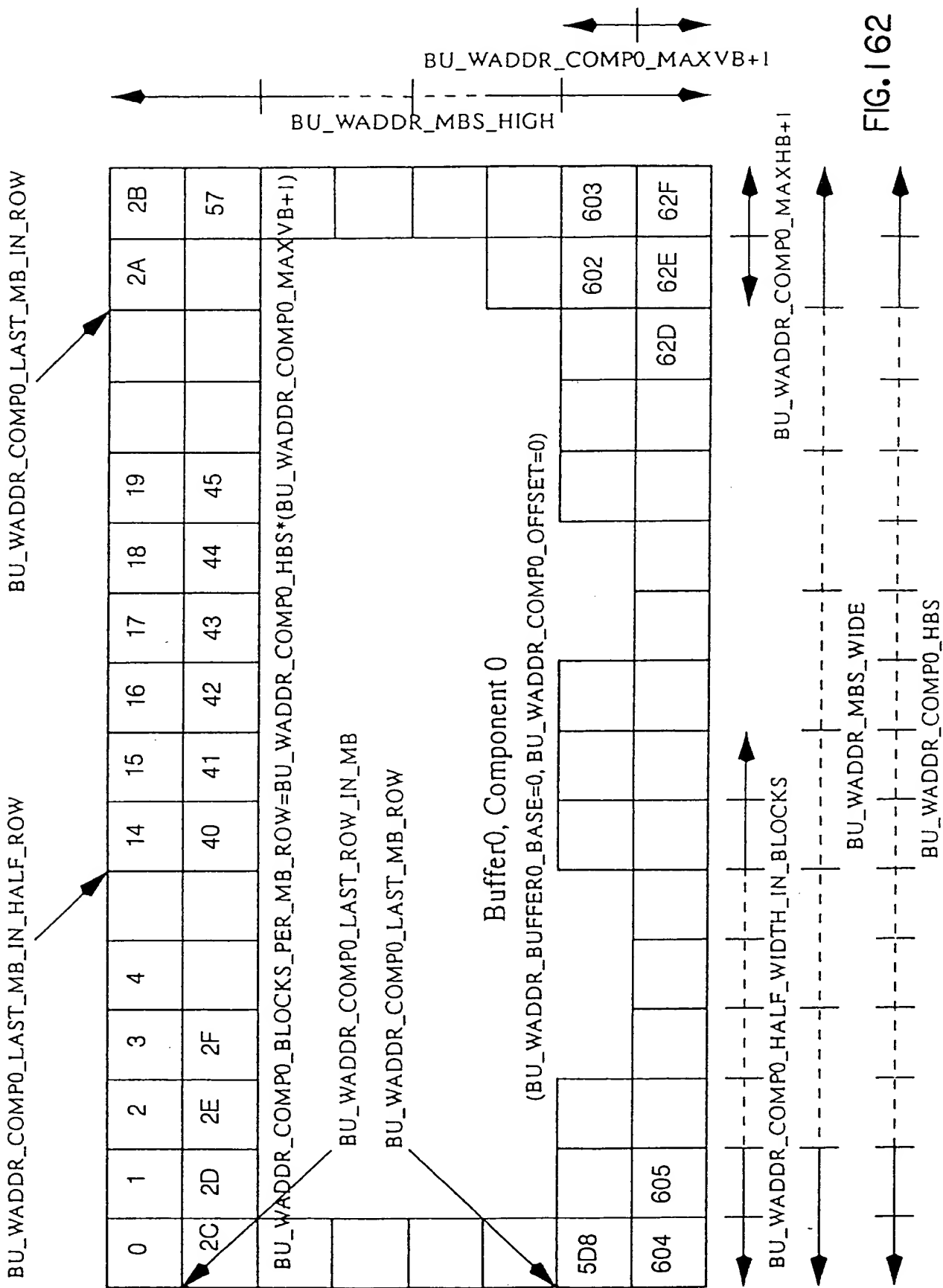
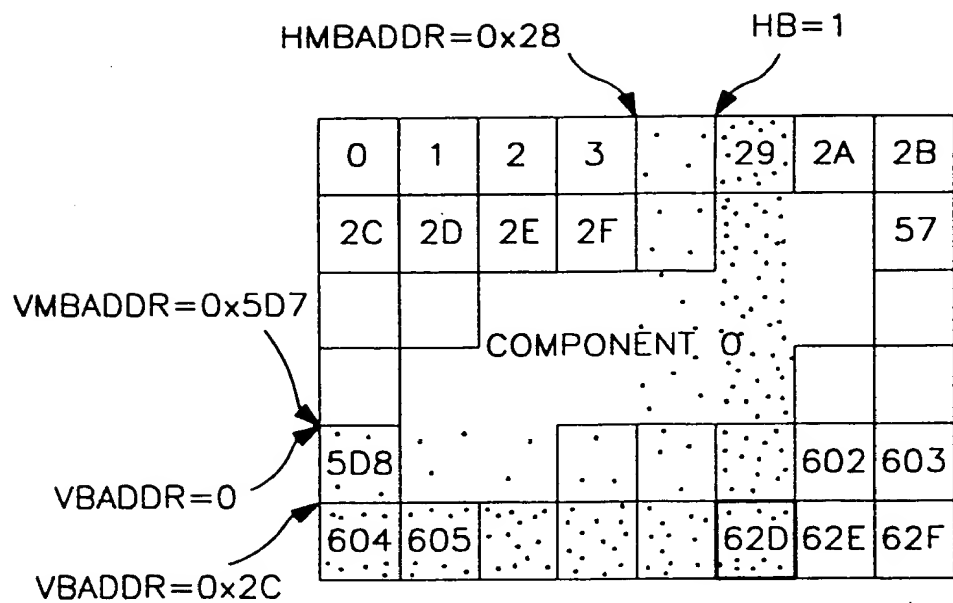
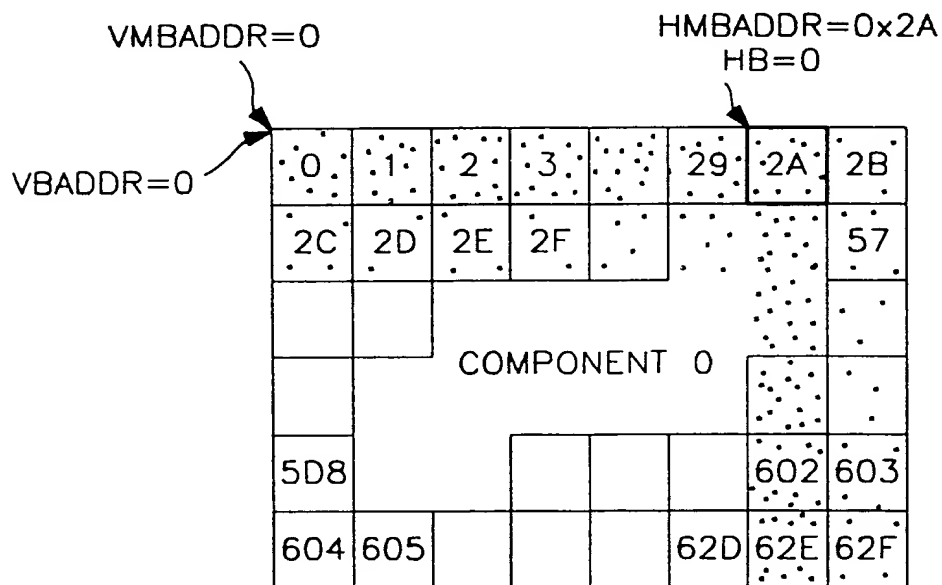


FIG. 162



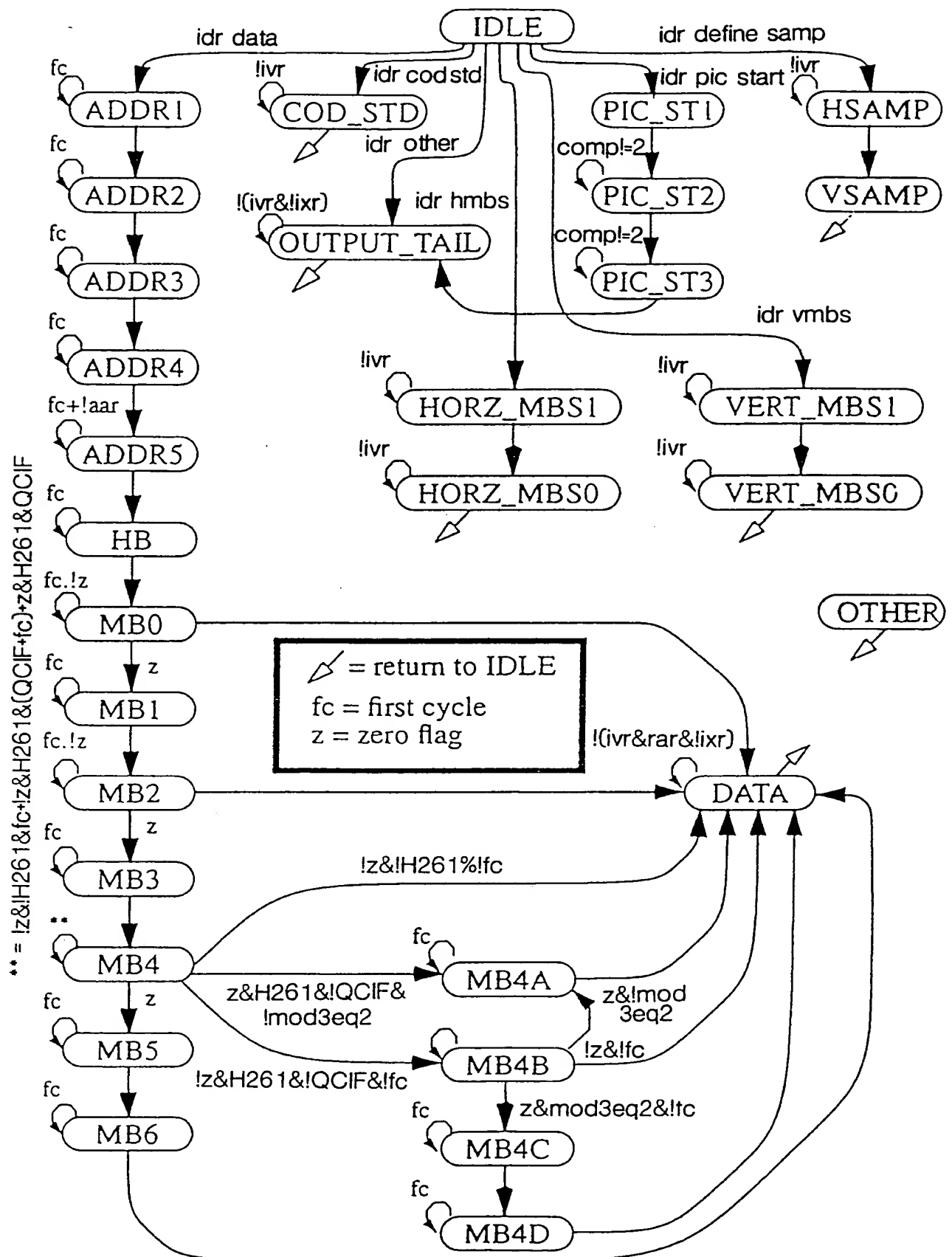
$$\text{BLOCK ADDRESS} = 0 + 0 + 0x5D8 + 0x28 + 0x2C + 1 = 0x62D$$

FIG. 163A



$$\text{BLOCK ADDRESS} = 0 + 0 + 0 + 0x2A + 0 + 0 = 0x2A$$

FIG. 163B



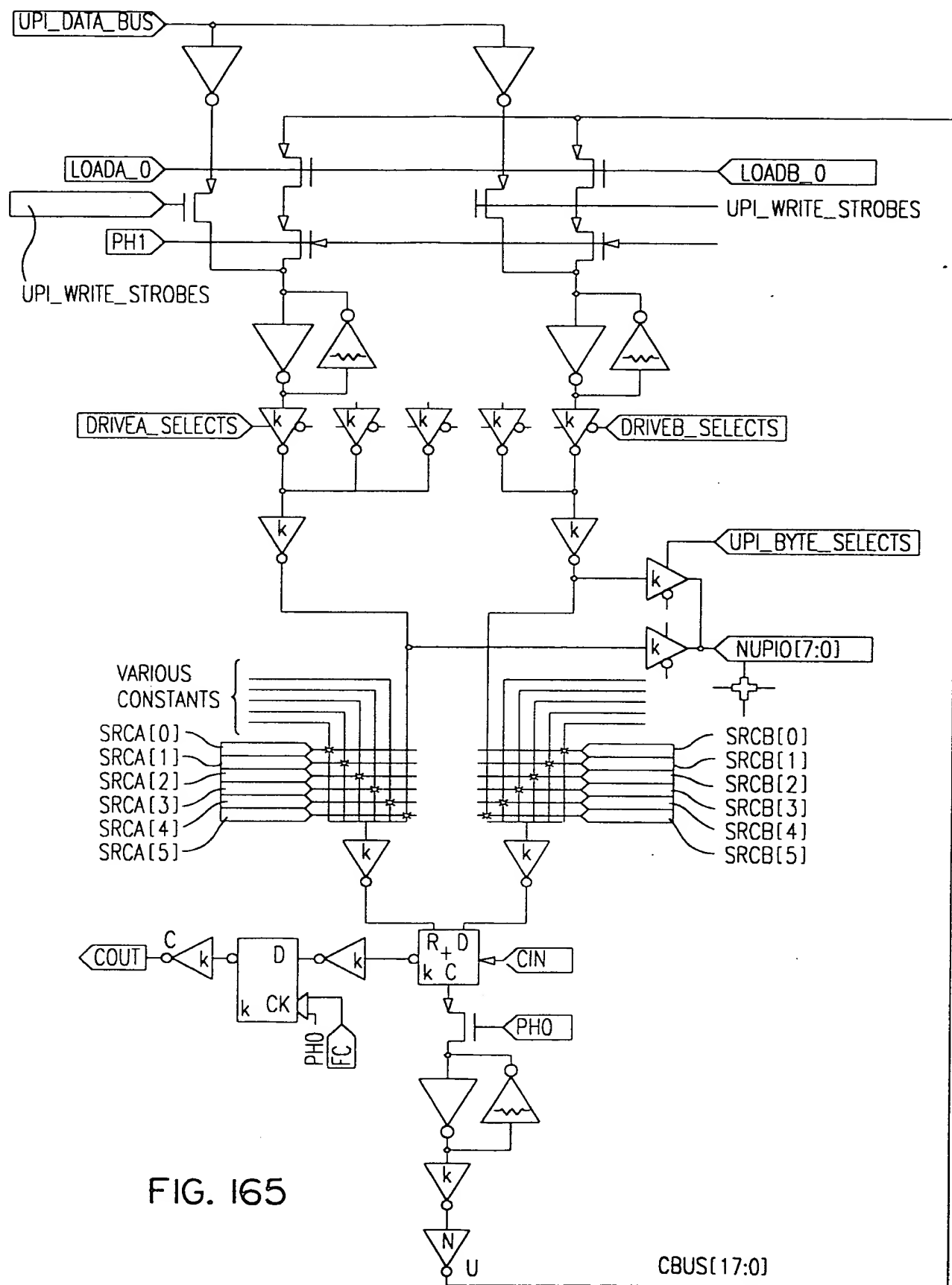
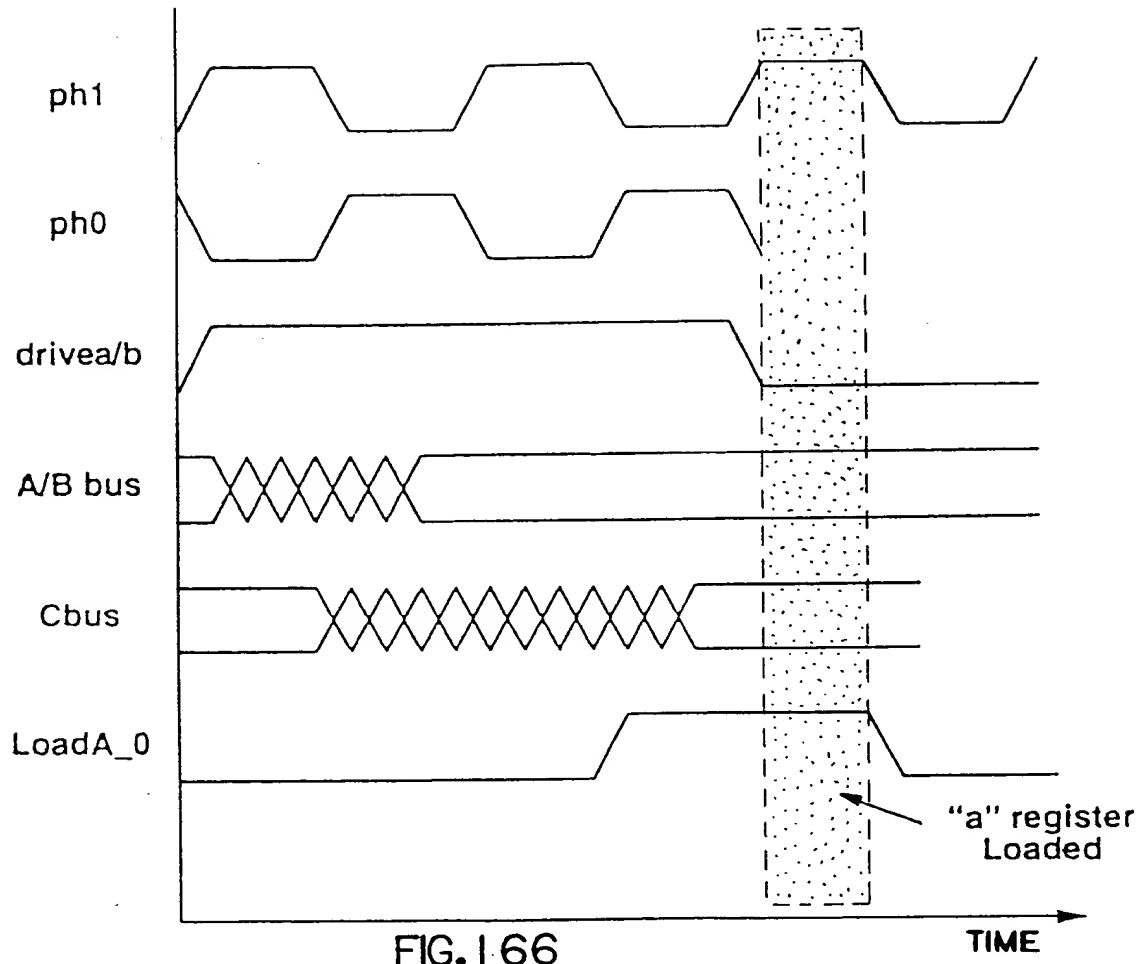


FIG. 165



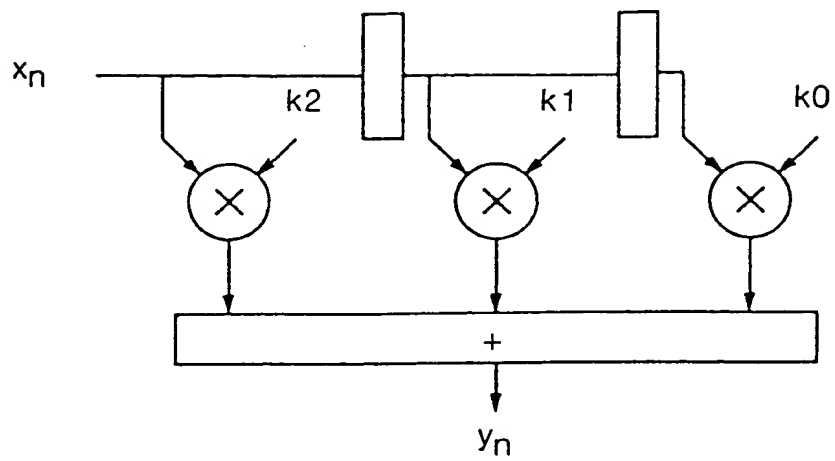


FIG. 167

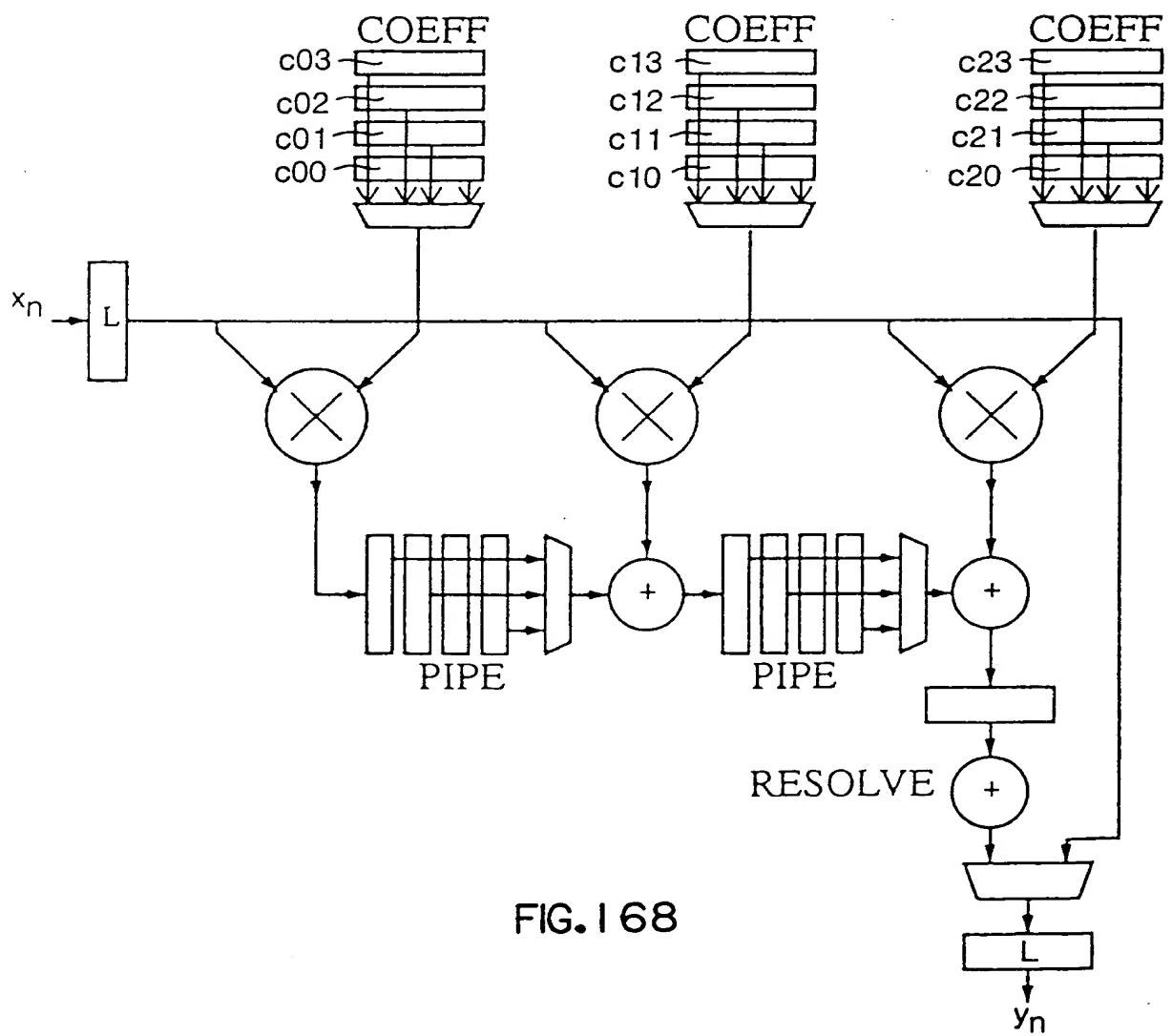


FIG. 168

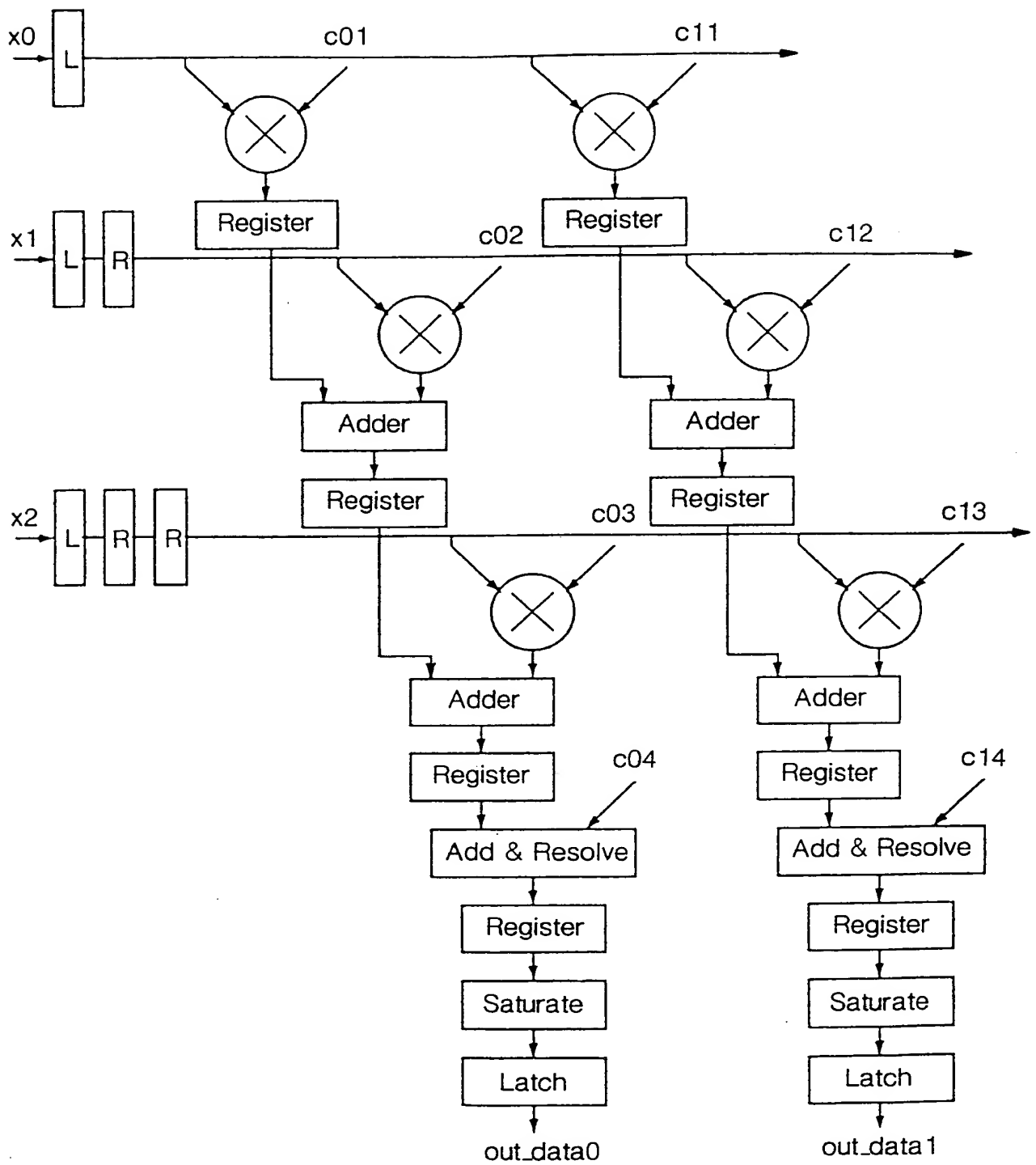


FIG. 1 69